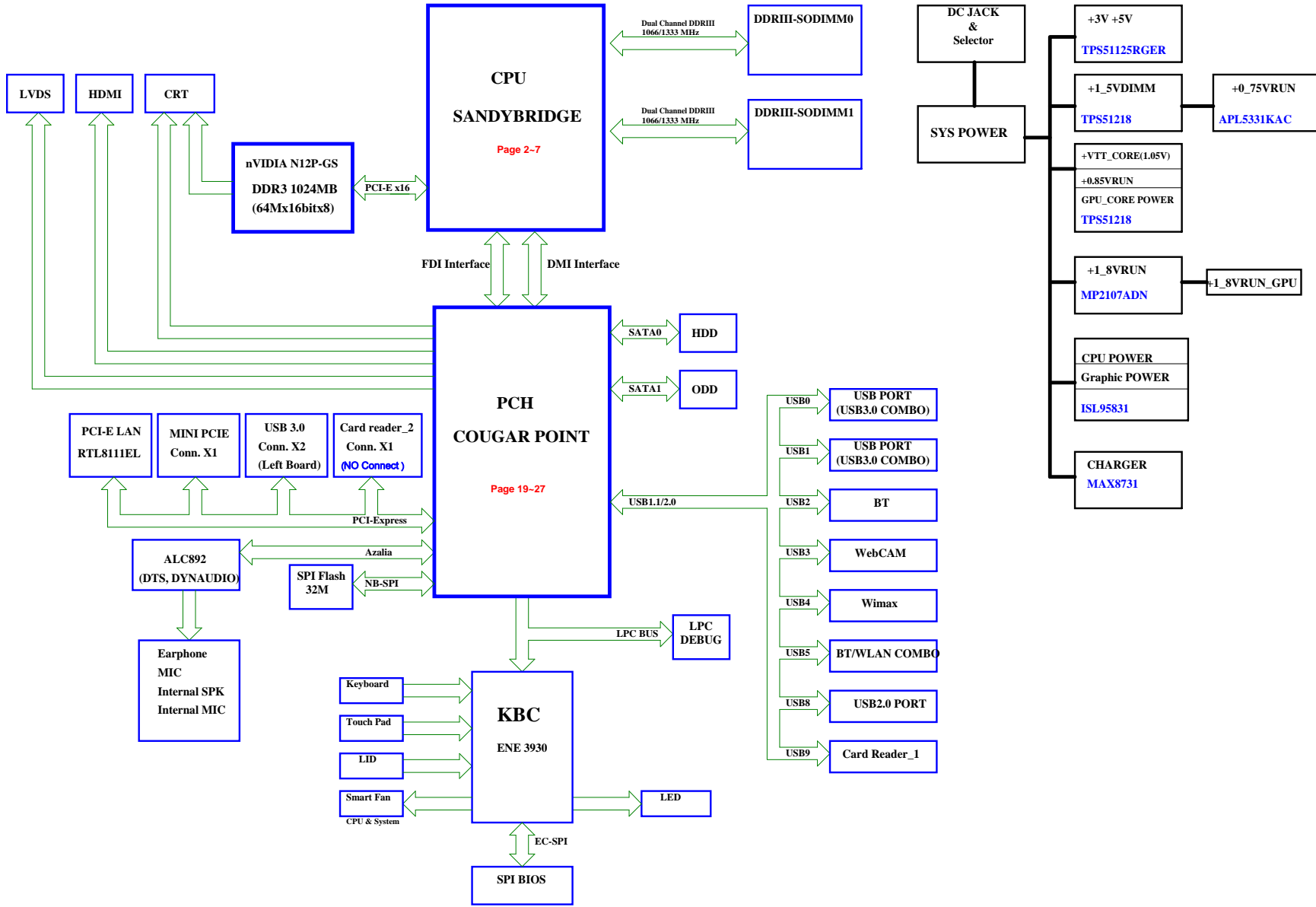


Huron River Platform

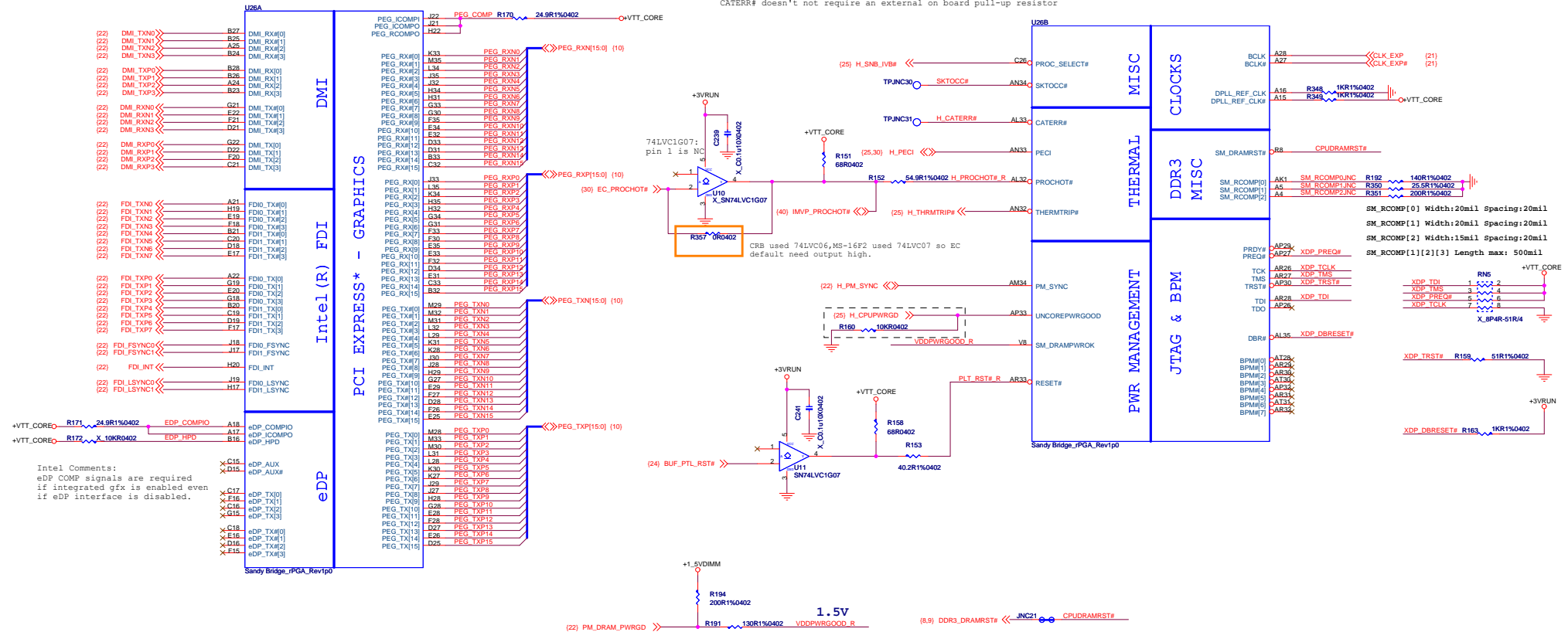
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09	DDR3 SODIMM 1
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11	nVIDIA N12P-GS_MEM Interface A
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13	nVIDIA N12P-GS_FrameA DDR3 I
14	nVIDIA N12P-GS_FrameA DDR3 II
15	nVIDIA N12P-GS_FrameC DDR3 I
16	nVIDIA N12P-GS_FrameC DDR3 II
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35	M_System Power
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38	M_0.85VRUN & 1.8VRUN
39	M_GPU CORE
40	M_CPU power,Graphic power
41	Screw / ME
42	EMI
43	[A] CRT/USB/LAN/BT/CONN
44	[A] PCIe GLAN(RTL 8111E)
45	[B] AUDIO/CONN
46	[B] USB3.0
47	[C] PWR_SW /LED Launch Board



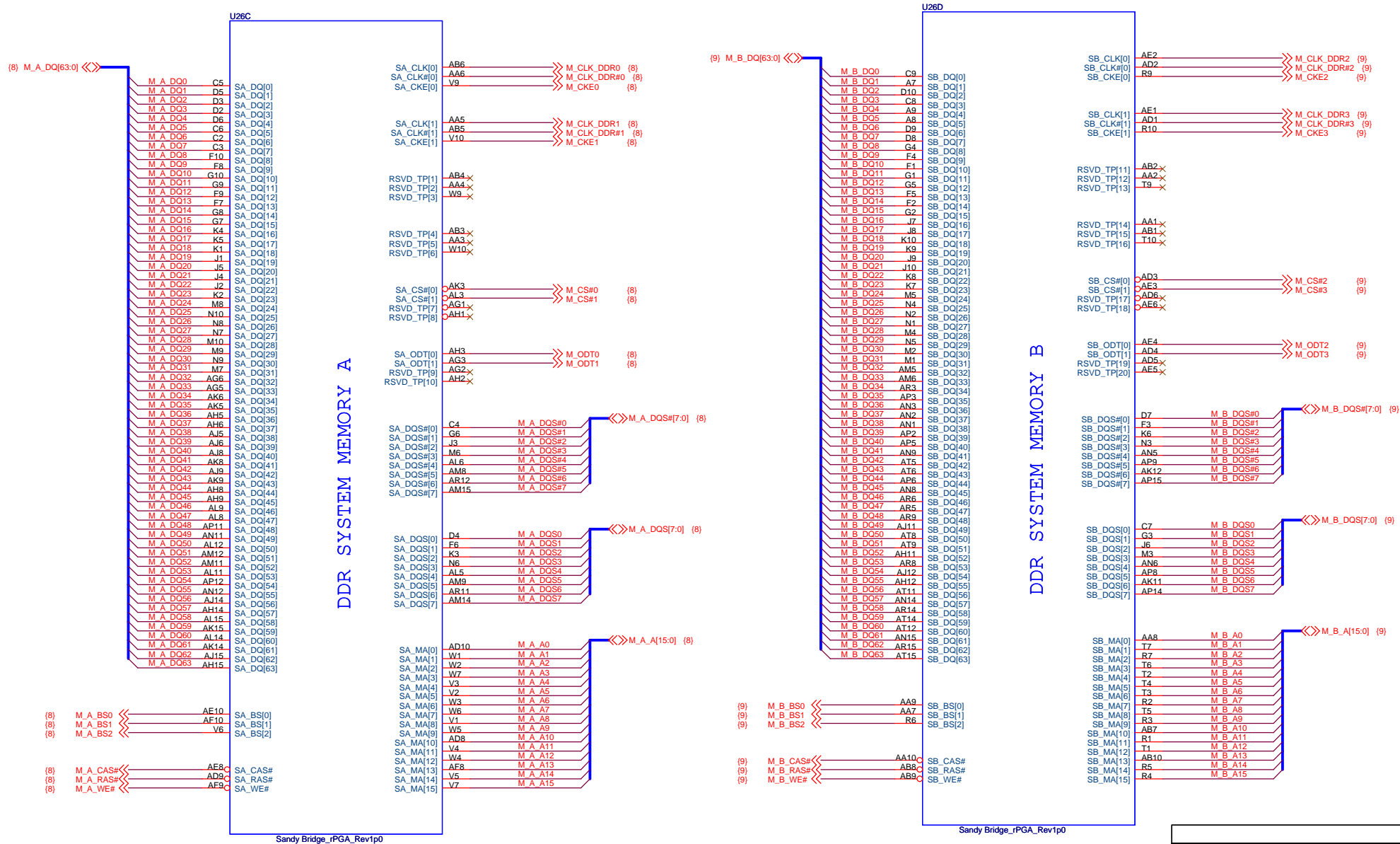
SANDYBRIDGE PROCESSOR (CLK,MISC,JTAG)

Intel Comments:
CATERR# doesn't not require an external on board pull-up resistor



Title										PROCESSOR-1 (HOST BUS)													
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SANDYBRIDGE PROCESSOR (DDR3)



SANDYBRIDGE PROCESSOR (POWER)

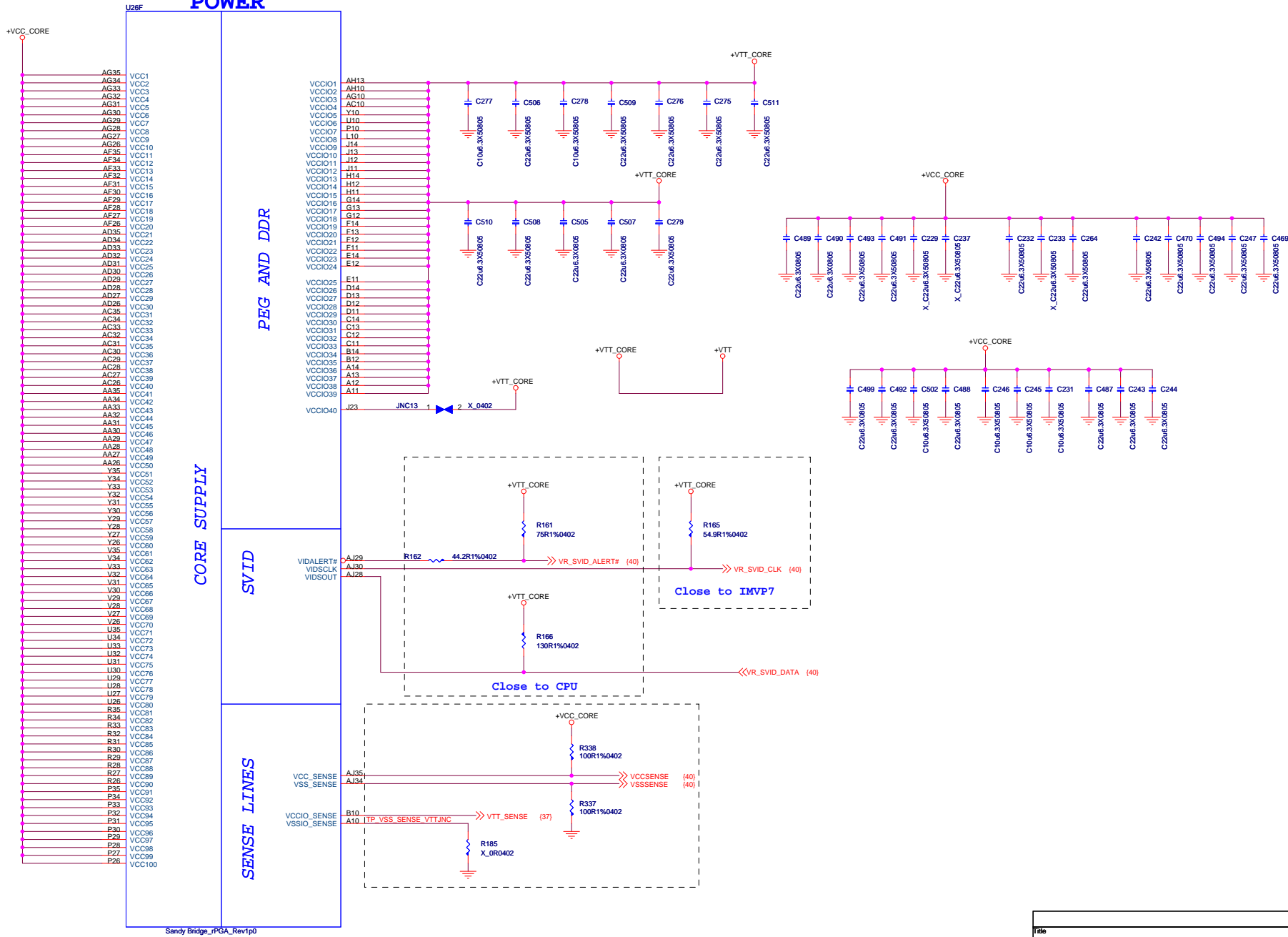
POWER

PEG AND DDR

CORE SUPPLY

SVID

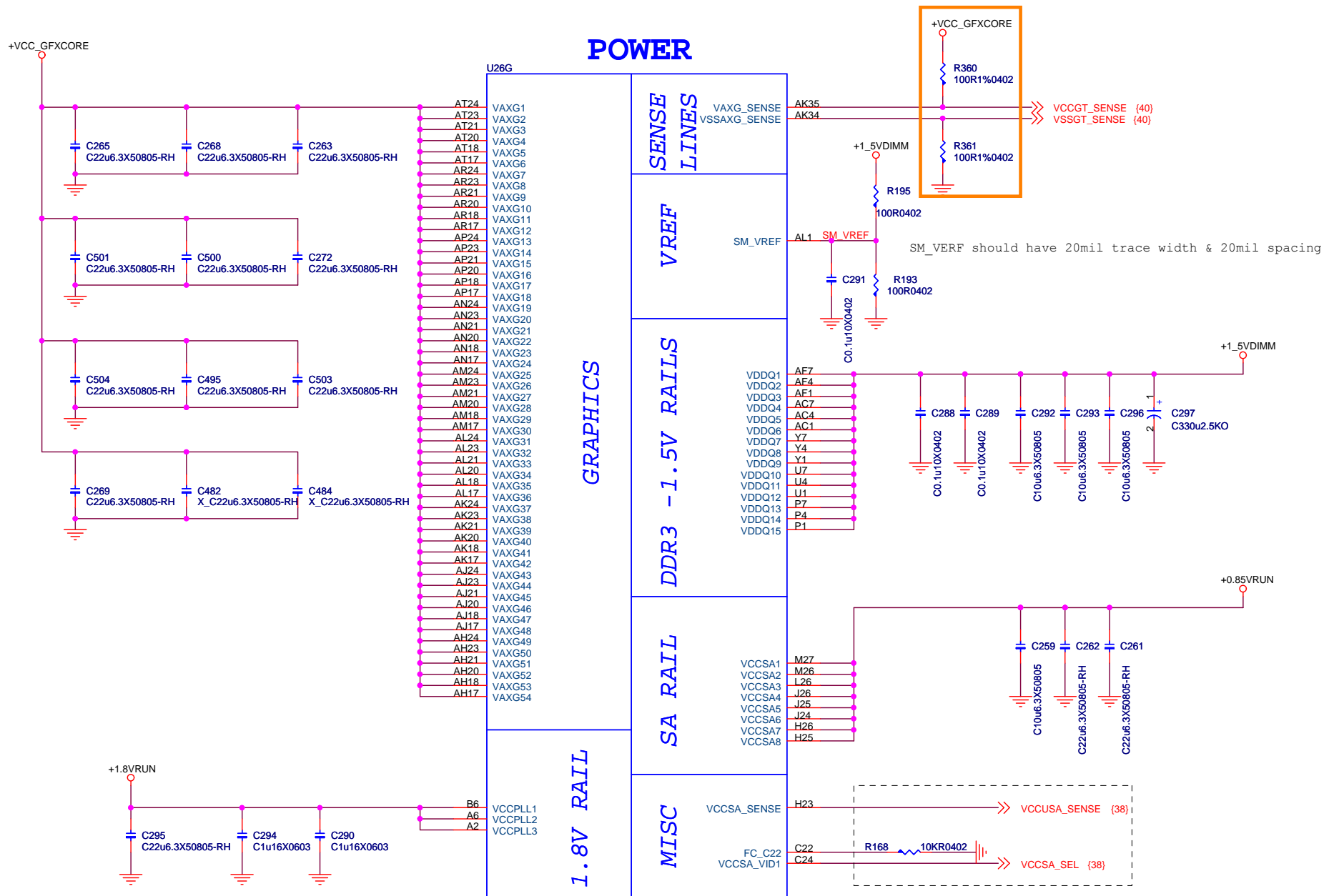
SENSE LINES



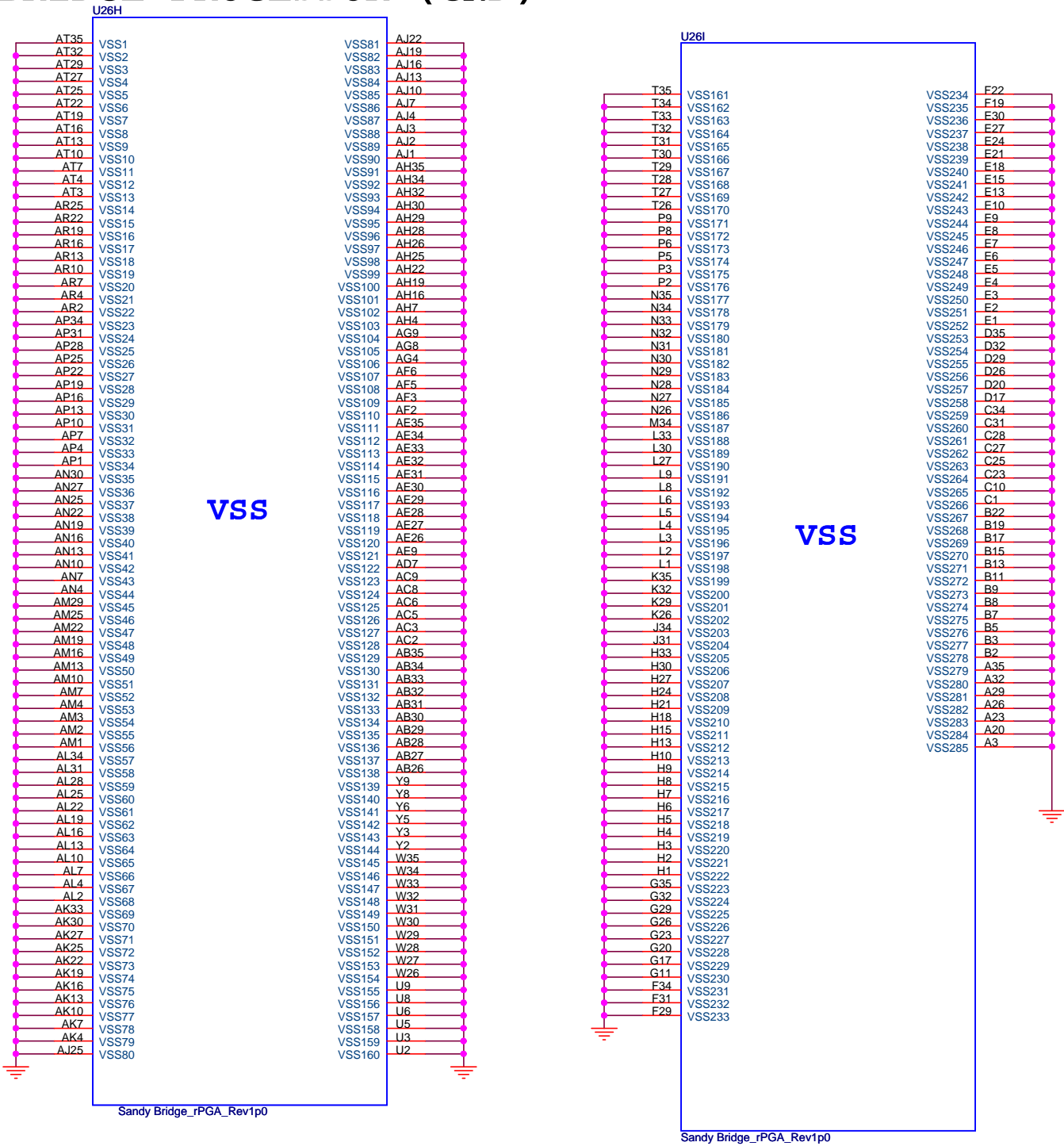
Sandy Bridge_PGA_Revip0

Title			
PROCESSOR-3 (POWER)			
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SANDYBRIDGE PROCESSOR (GRAPHICS POWER)



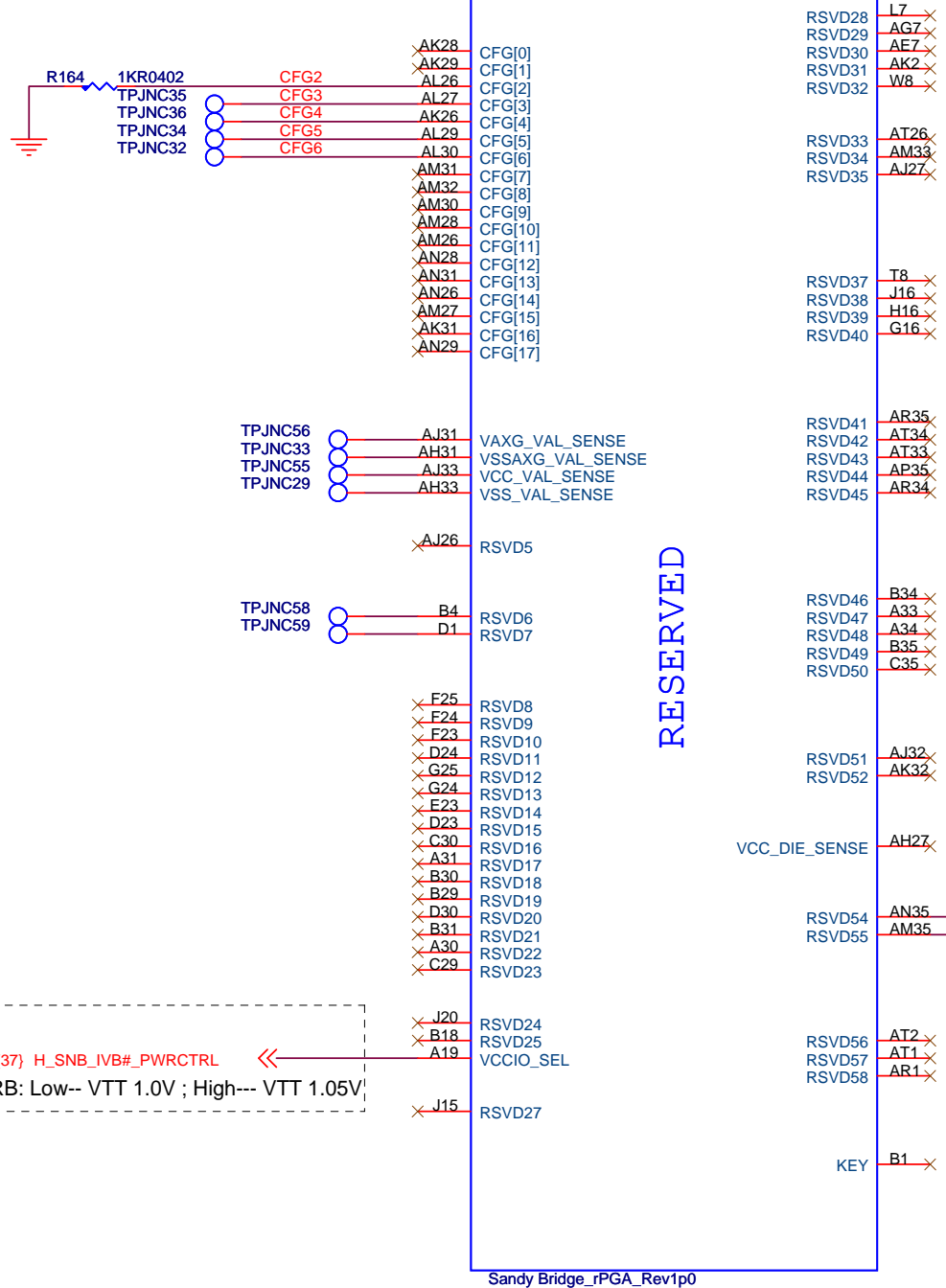
SANDYBRIDGE PROCESSOR (GND)



Title			
PROCESSOR-5 (GND)			
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SANDYBRIDGE PROCESSOR (RESERVED)

U26E



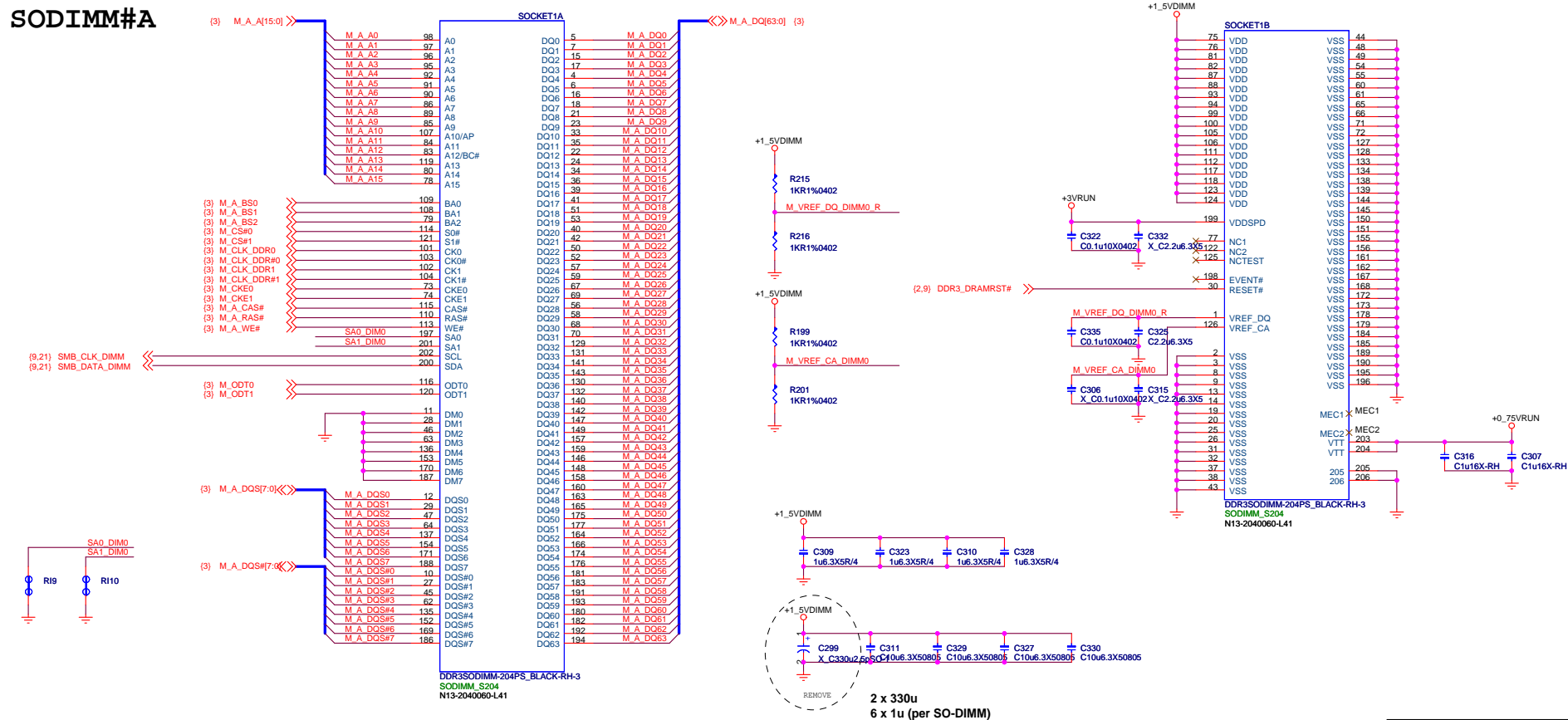
CFG3 - PCI-Express Static Lane Reversal	
CFG2	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

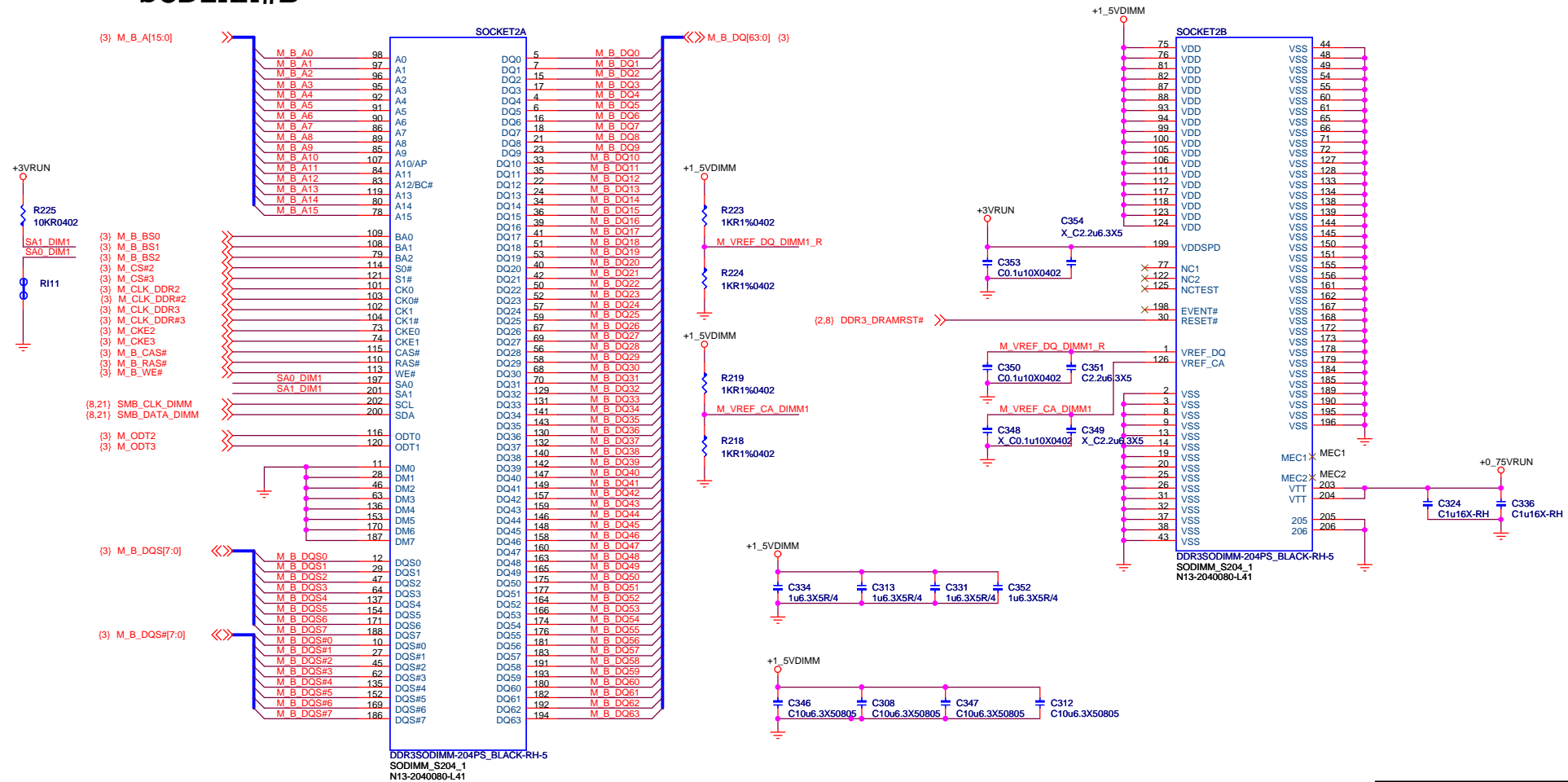
PCI-Express Configuration Select	
CFG[5:6]	11:Default X16-device 1 functions 1 and 2 disabled 10: X8 X8-device 1 functions 1 enable, function2 disabled 01:Reserved--(device 1 functions 1disabled function2 enable 00: X8 X4 X4-device 1 functions 1 and 2 enable

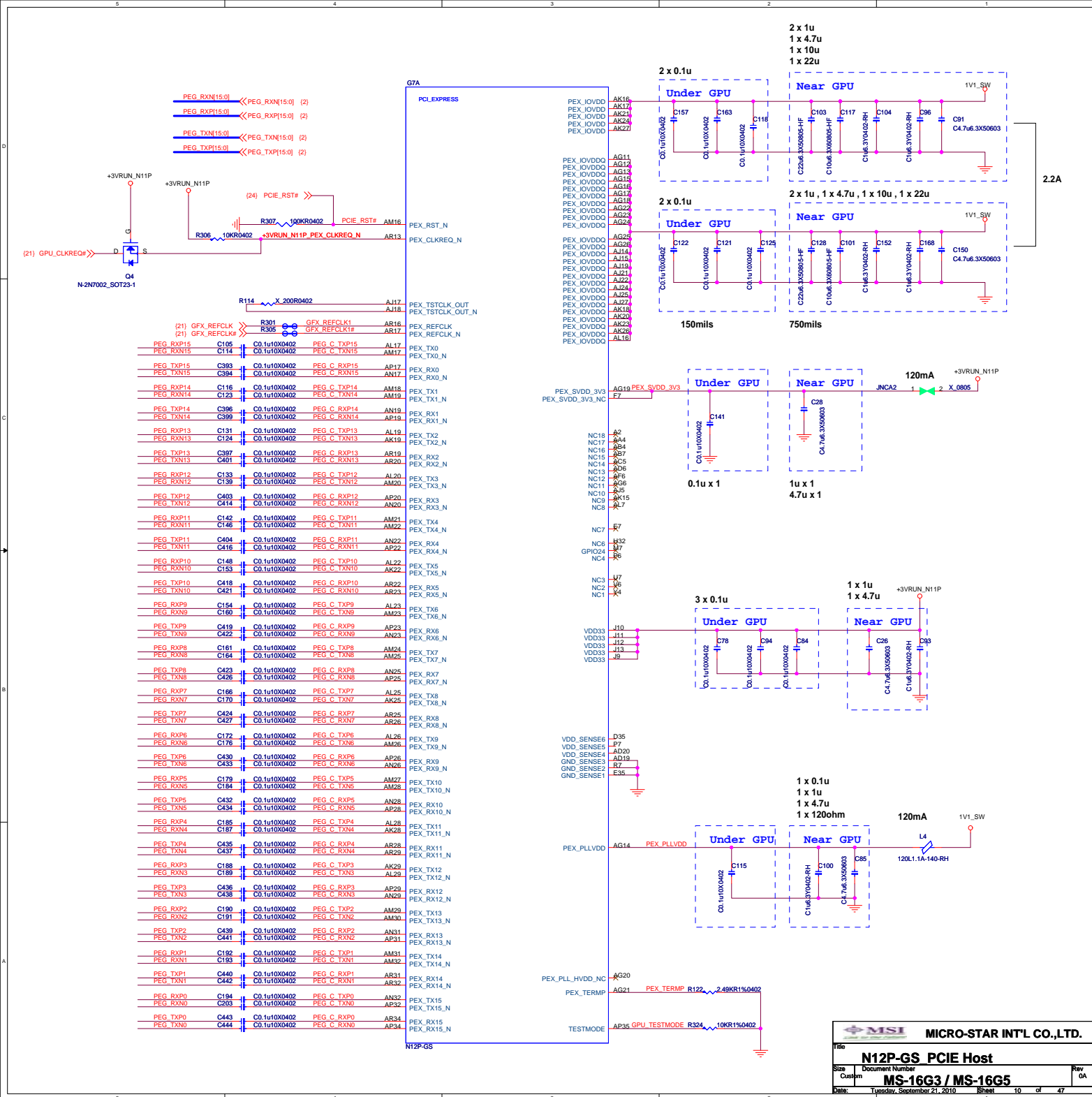
PROCESSOR-6 (RESERVE)		
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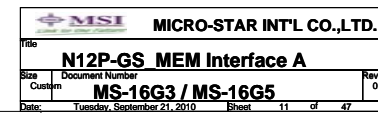
SODIMM#A

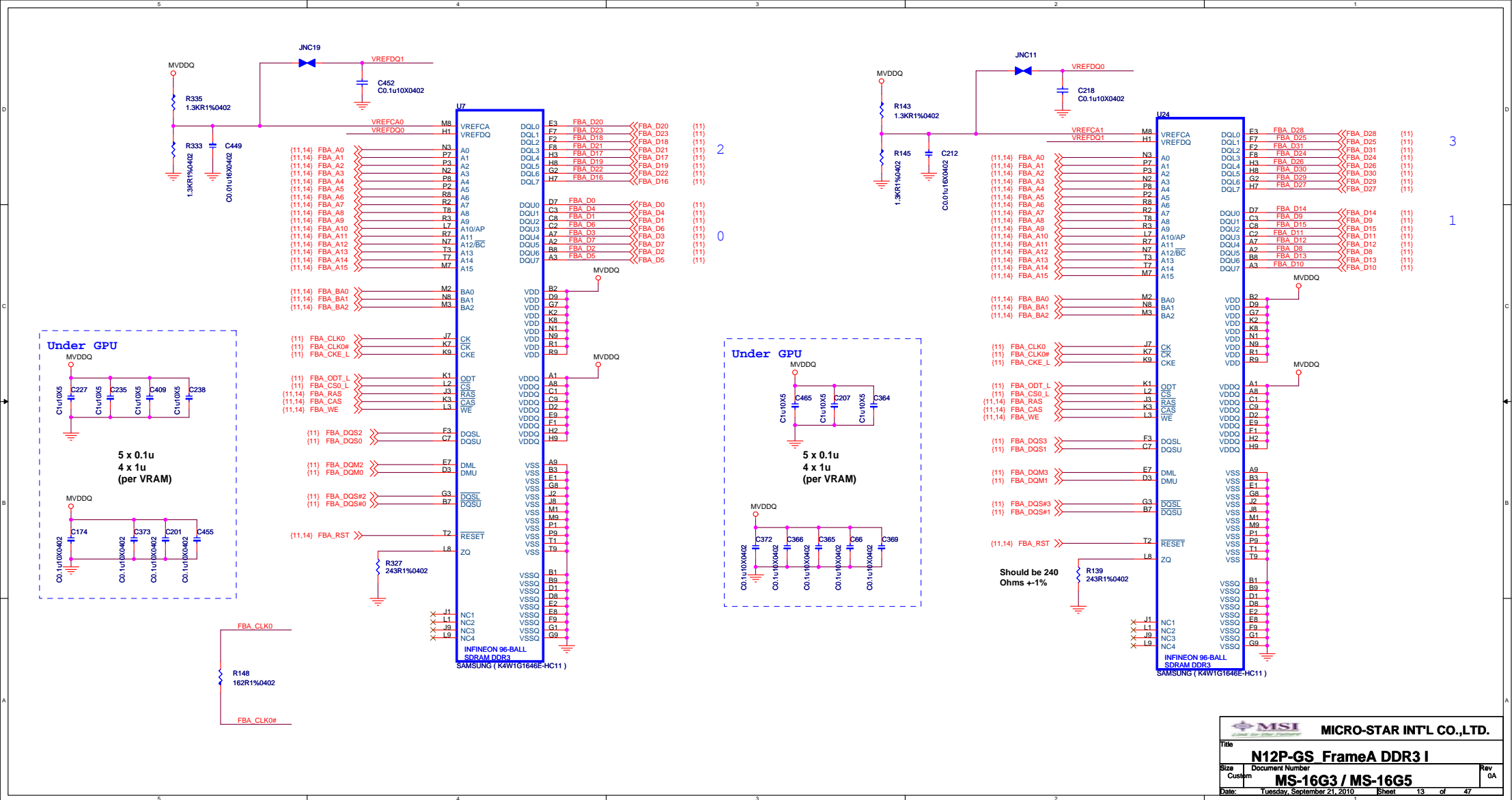


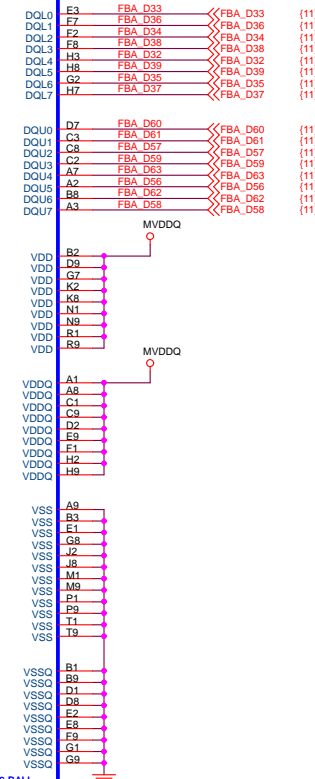
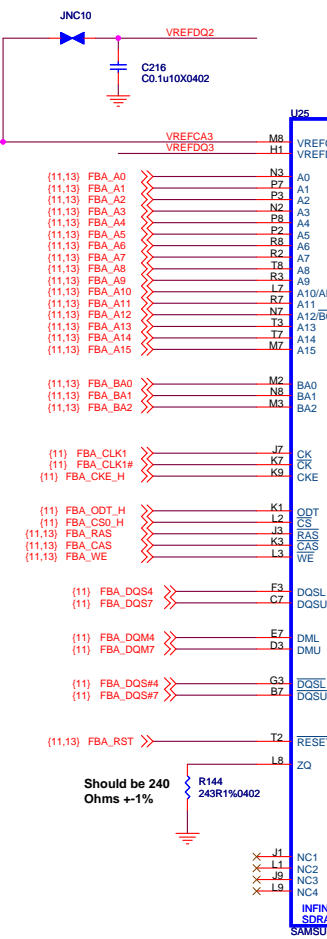
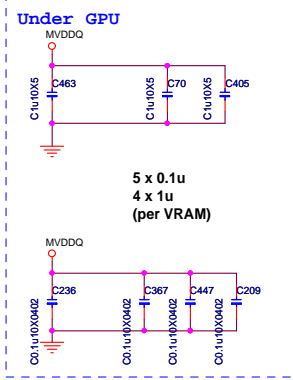
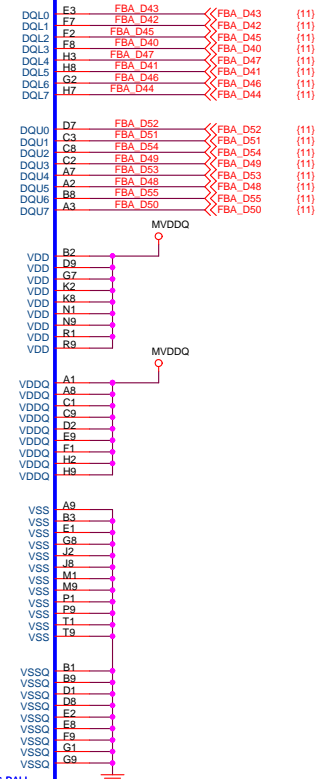
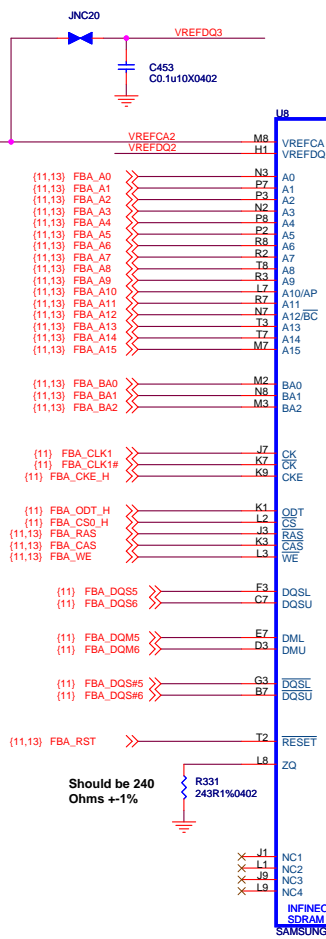
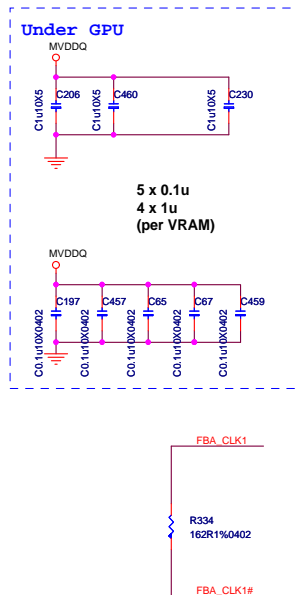
SODIMM#B

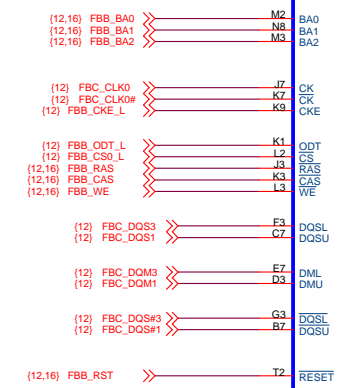
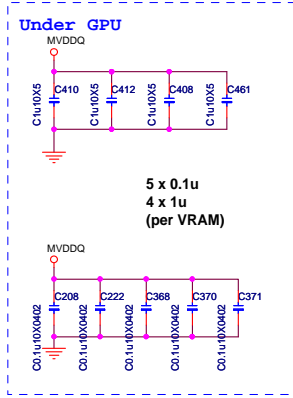
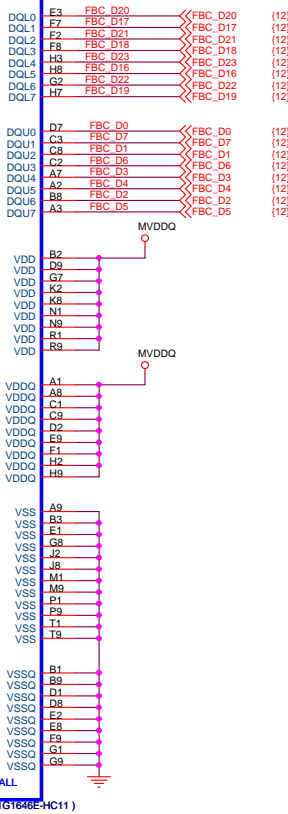
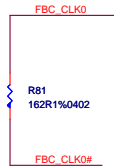
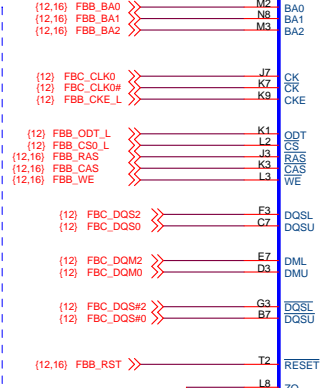
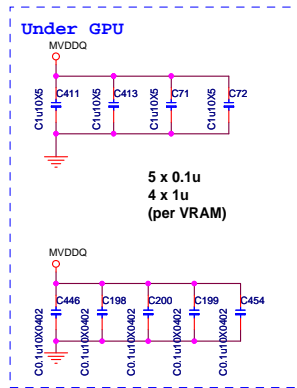




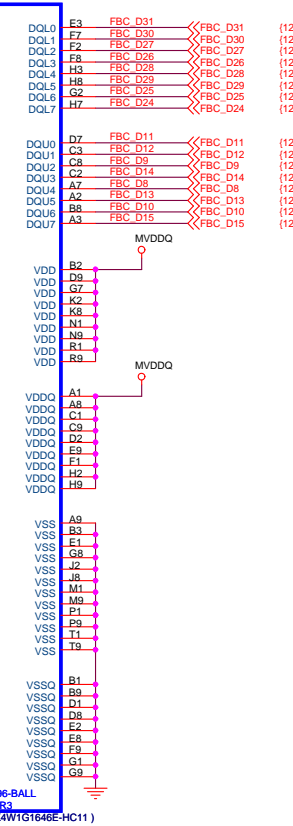


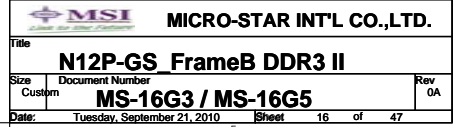


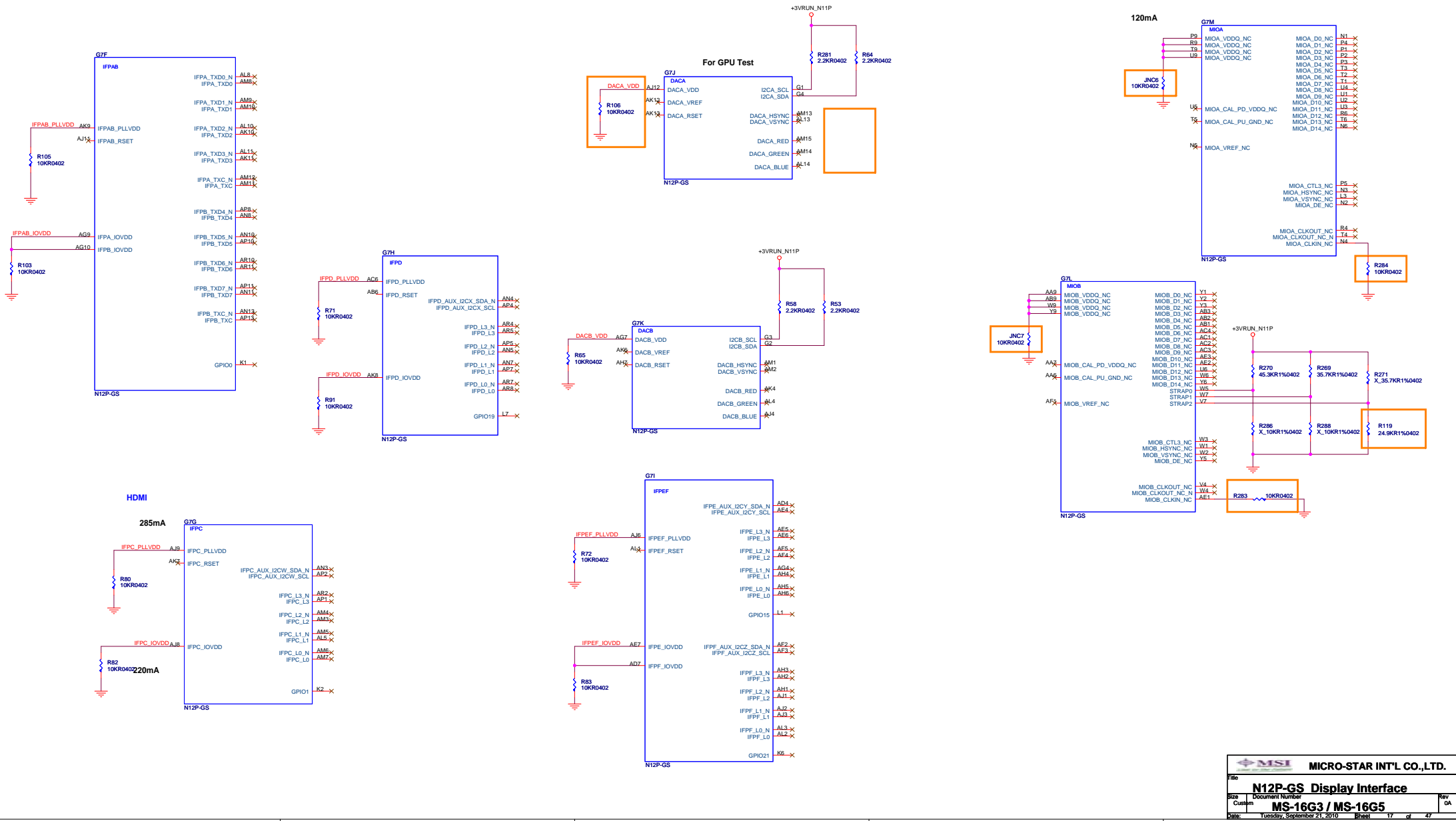


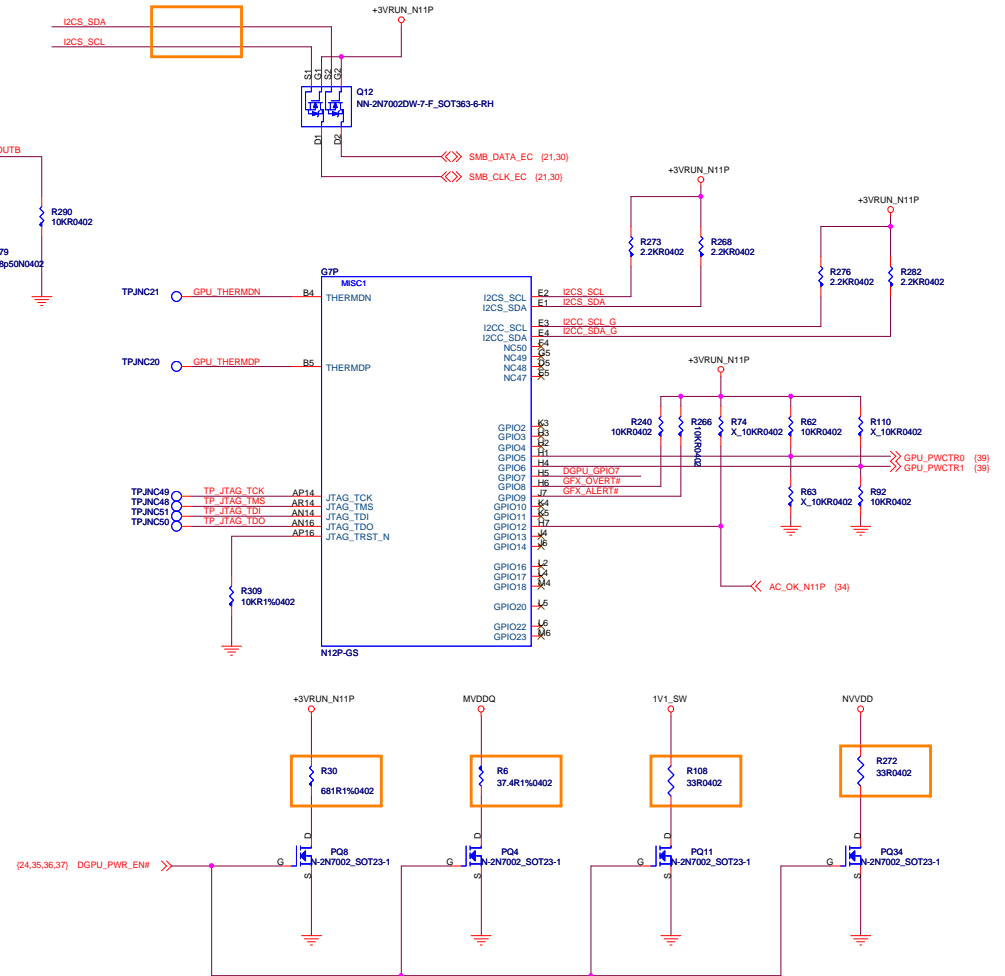
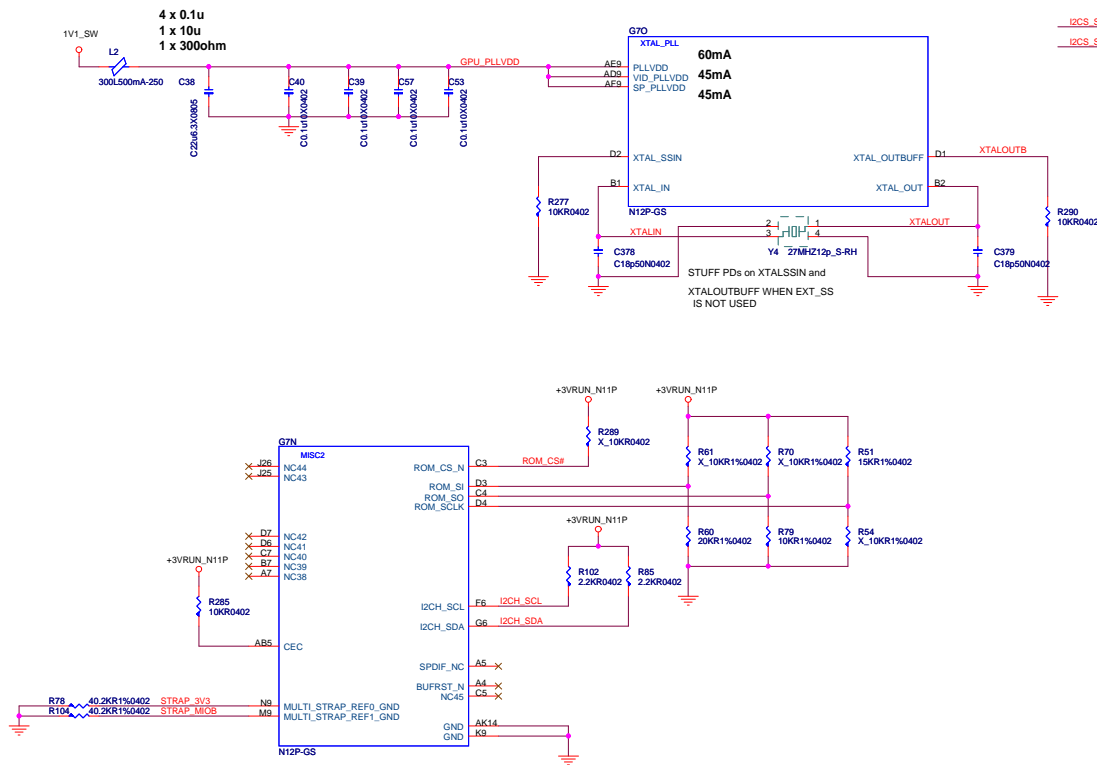


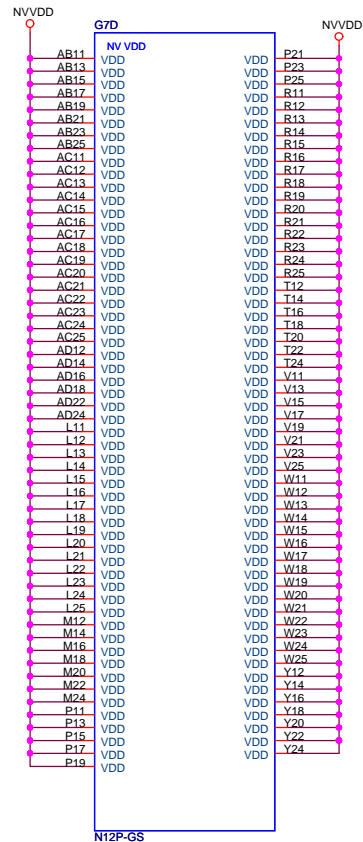
Should be 240
Ohms +-1%



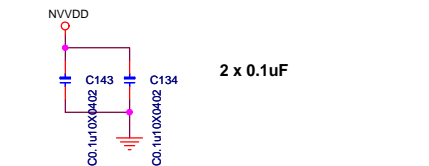
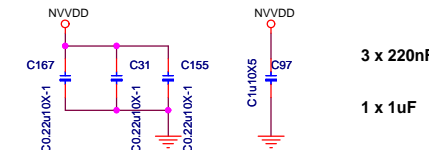
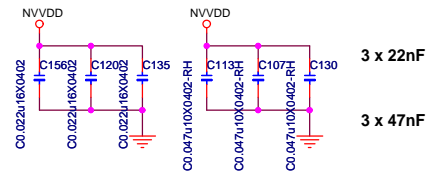
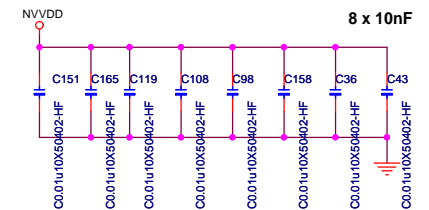




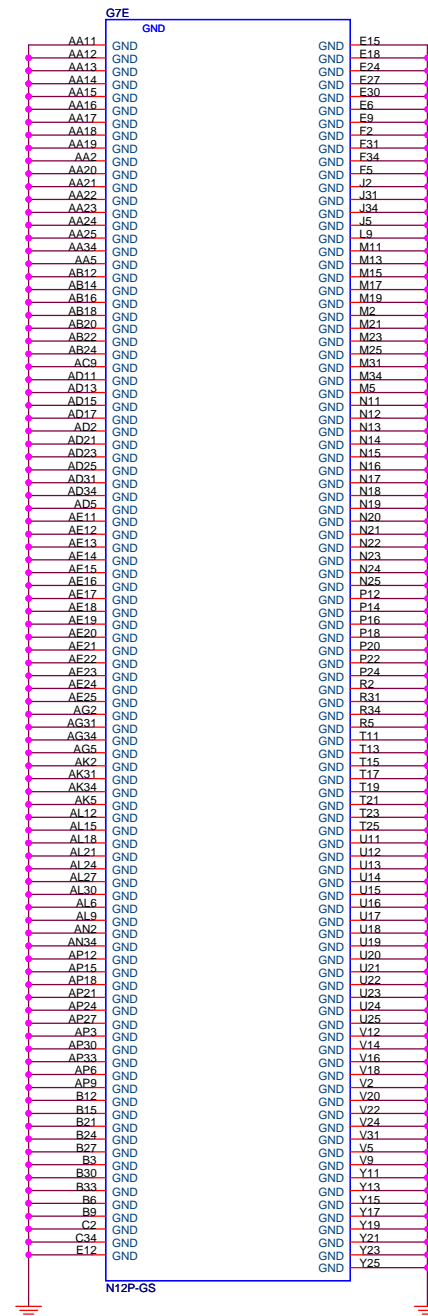
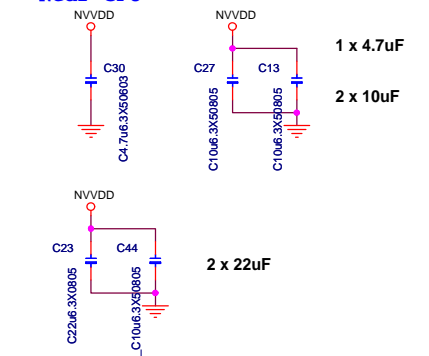




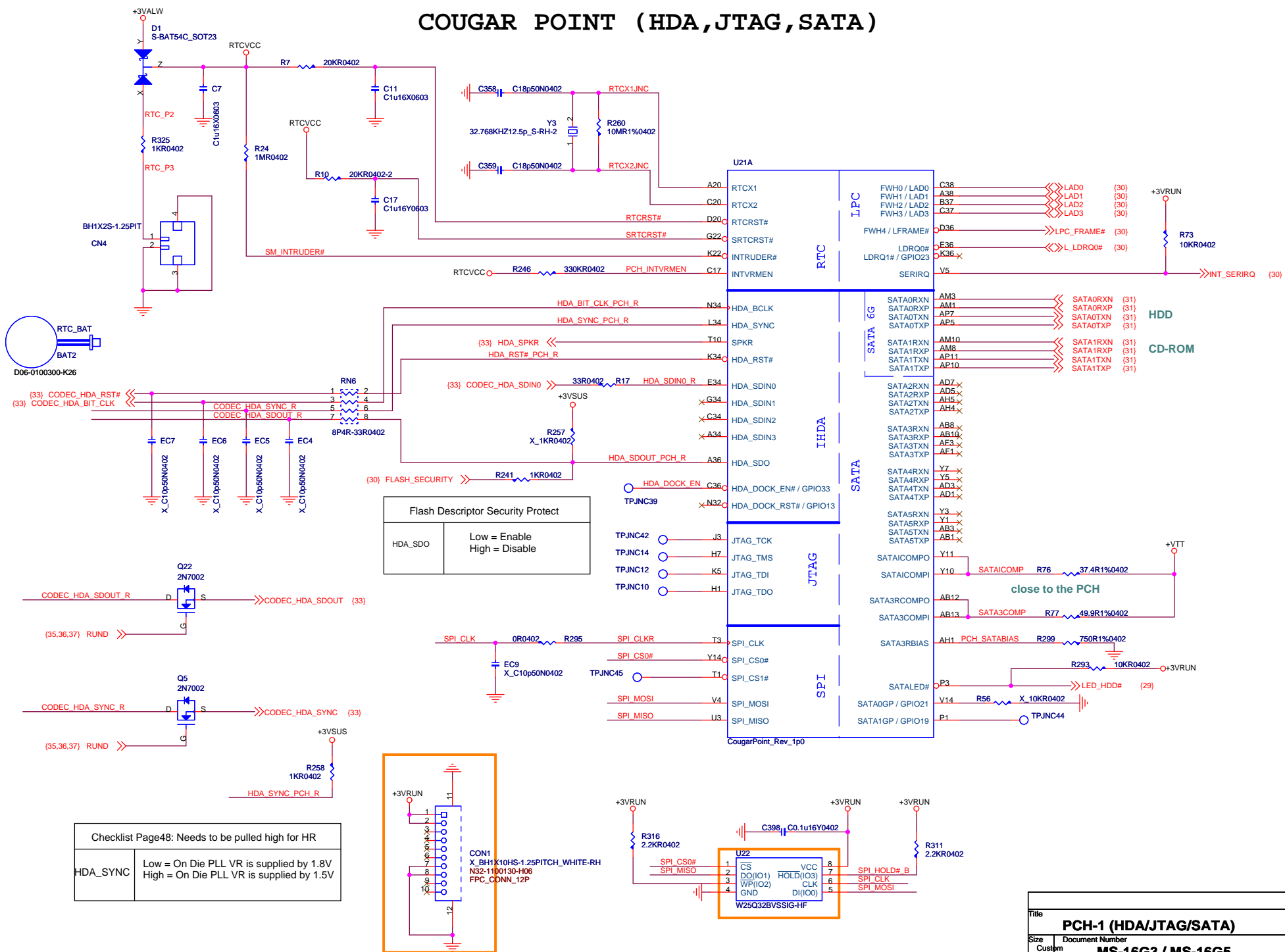
Under GPU



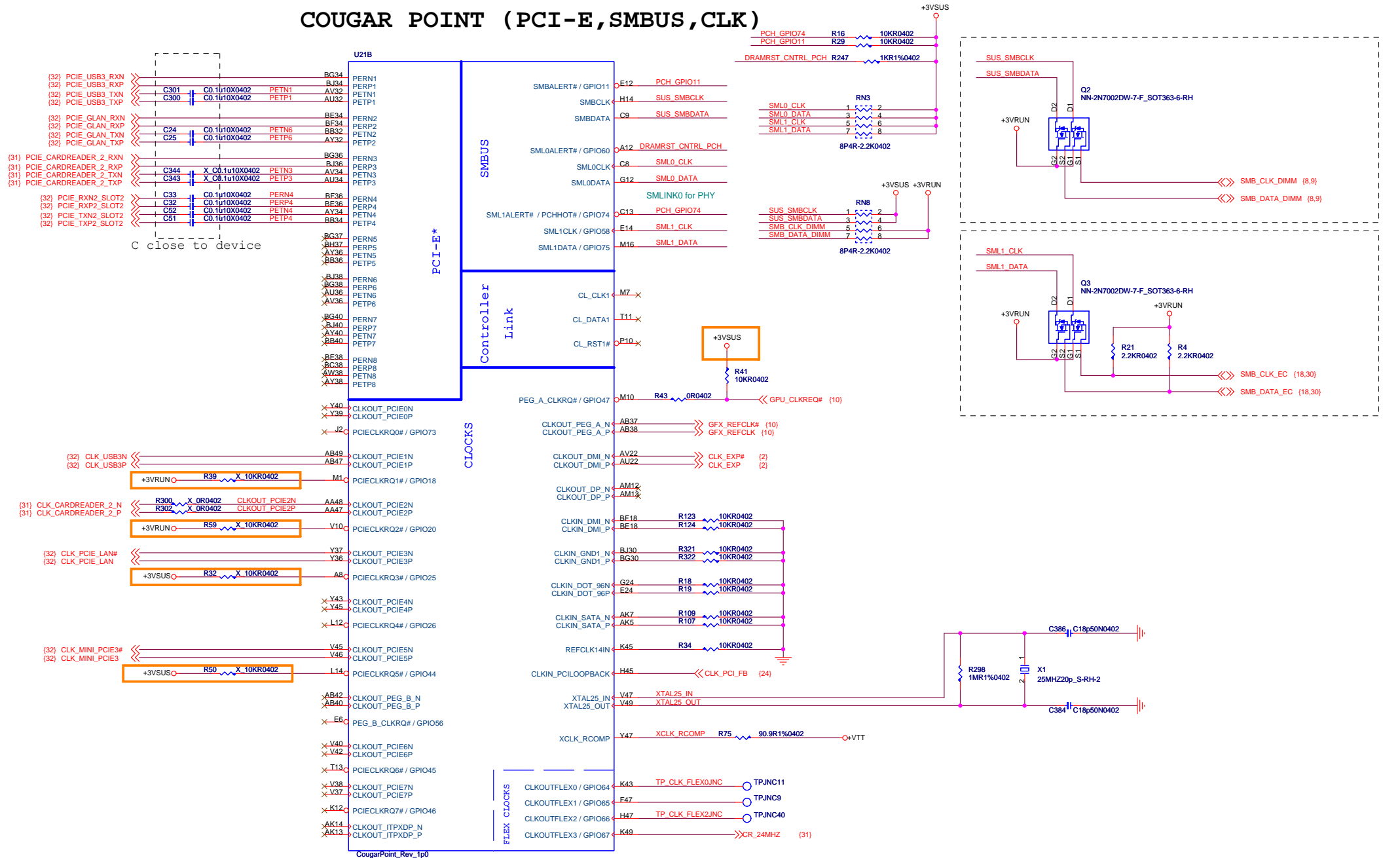
Near GPU



COUGAR POINT (HDA,JTAG,SATA)



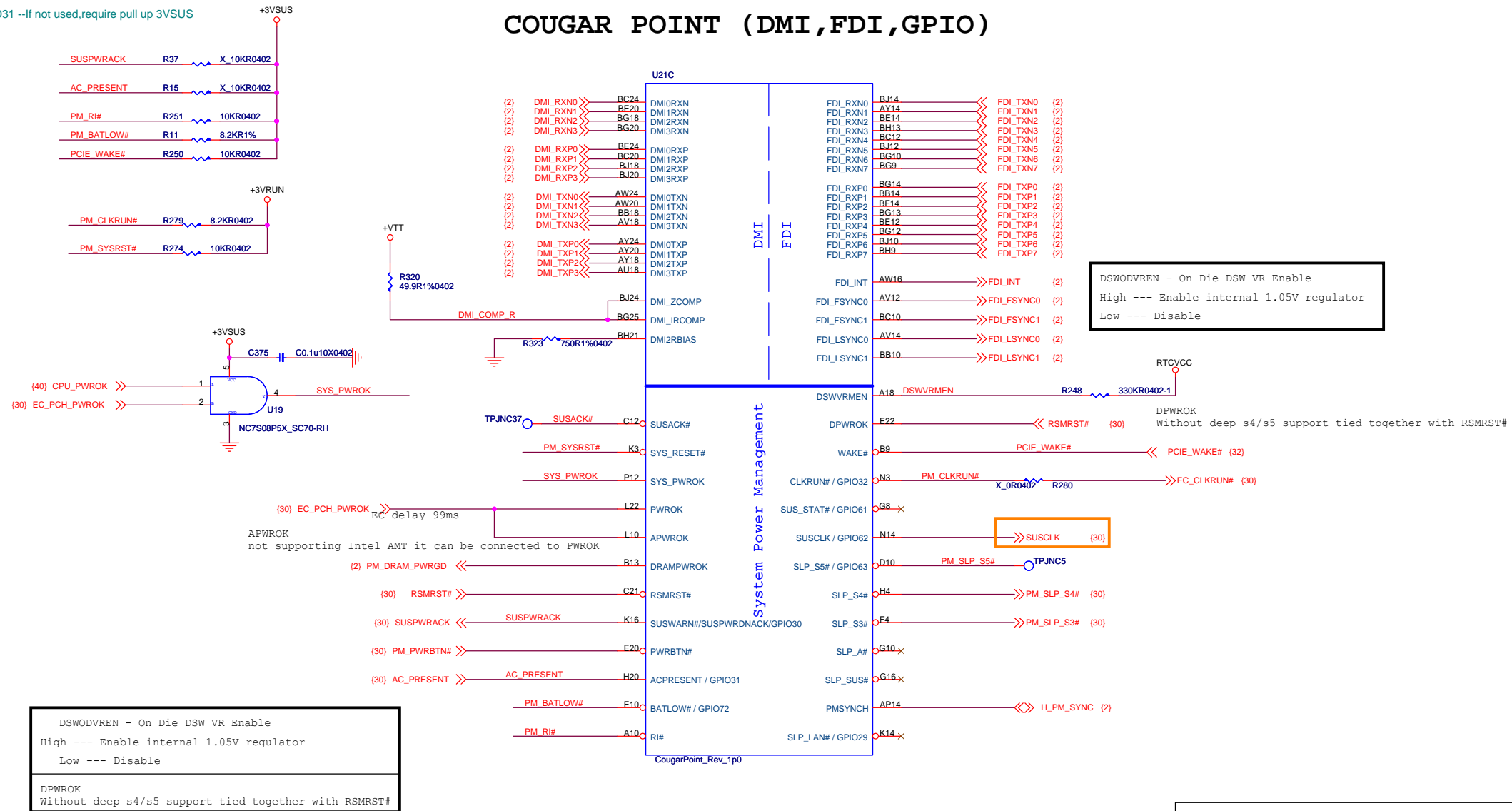
COUGAR POINT (PCI-E, SMBUS, CLK)



File		
PCH-2 (PCI-E/SMBUS/CLK)		
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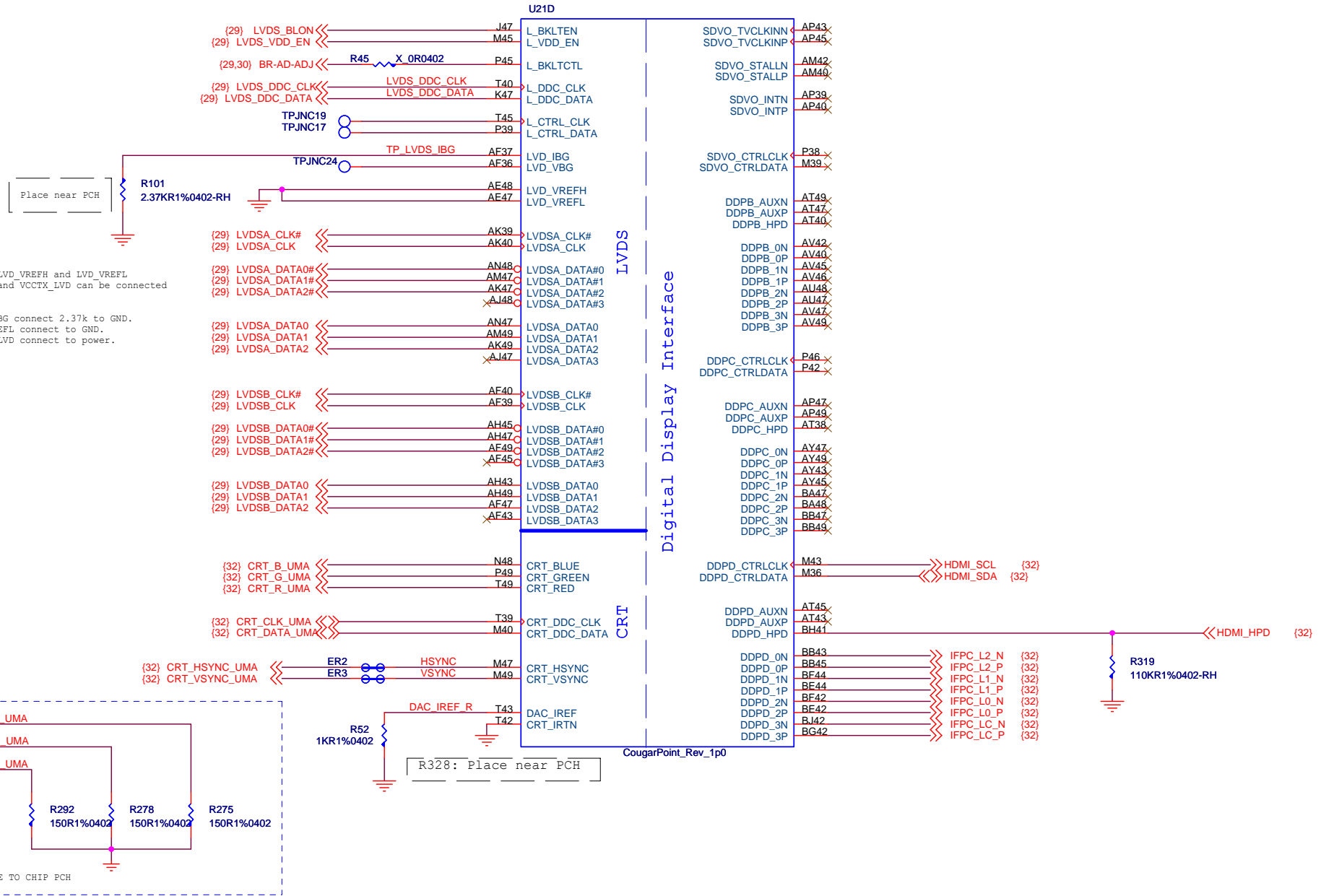
GPIO31 --If not used,require pull up 3VSUS

COUGAR POINT (DMI,FDI,GPIO)

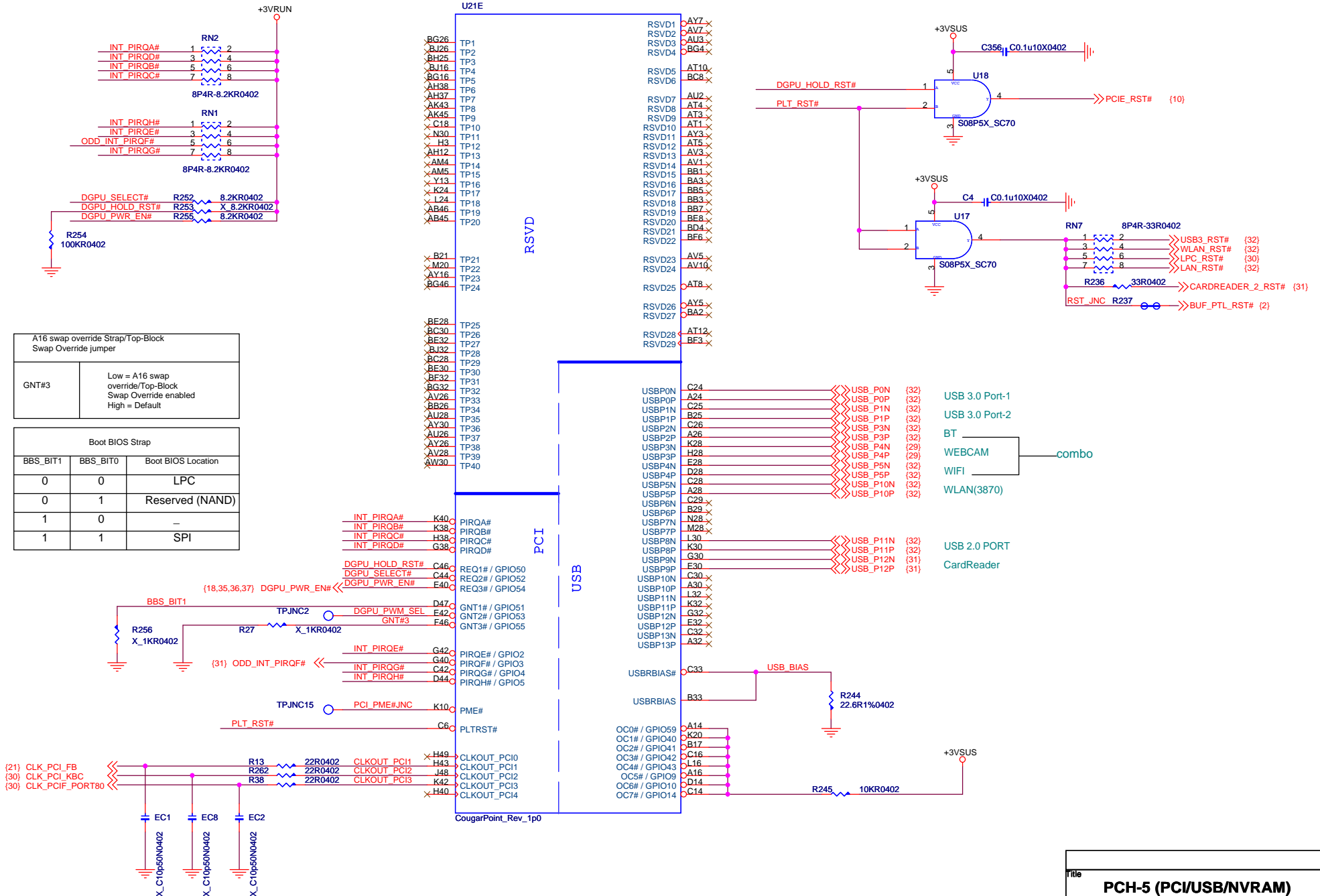


Title		
PCH-3 (DMI/FDI/GPIO)		
Size	Document Number	Rev
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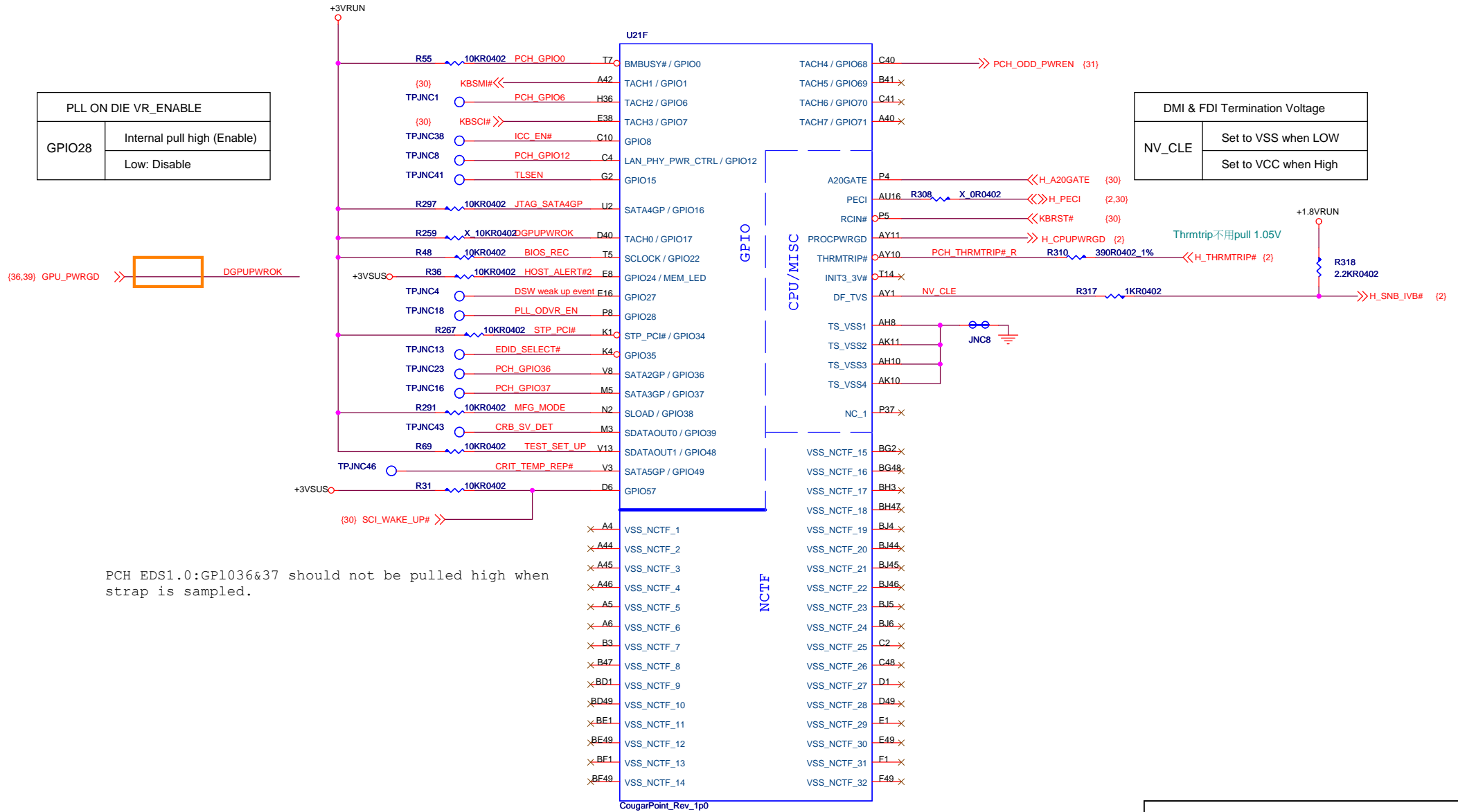
COUGAR POINT (LVDS,DDI)



COUGAR POINT (PCI,USB,NVRAM)

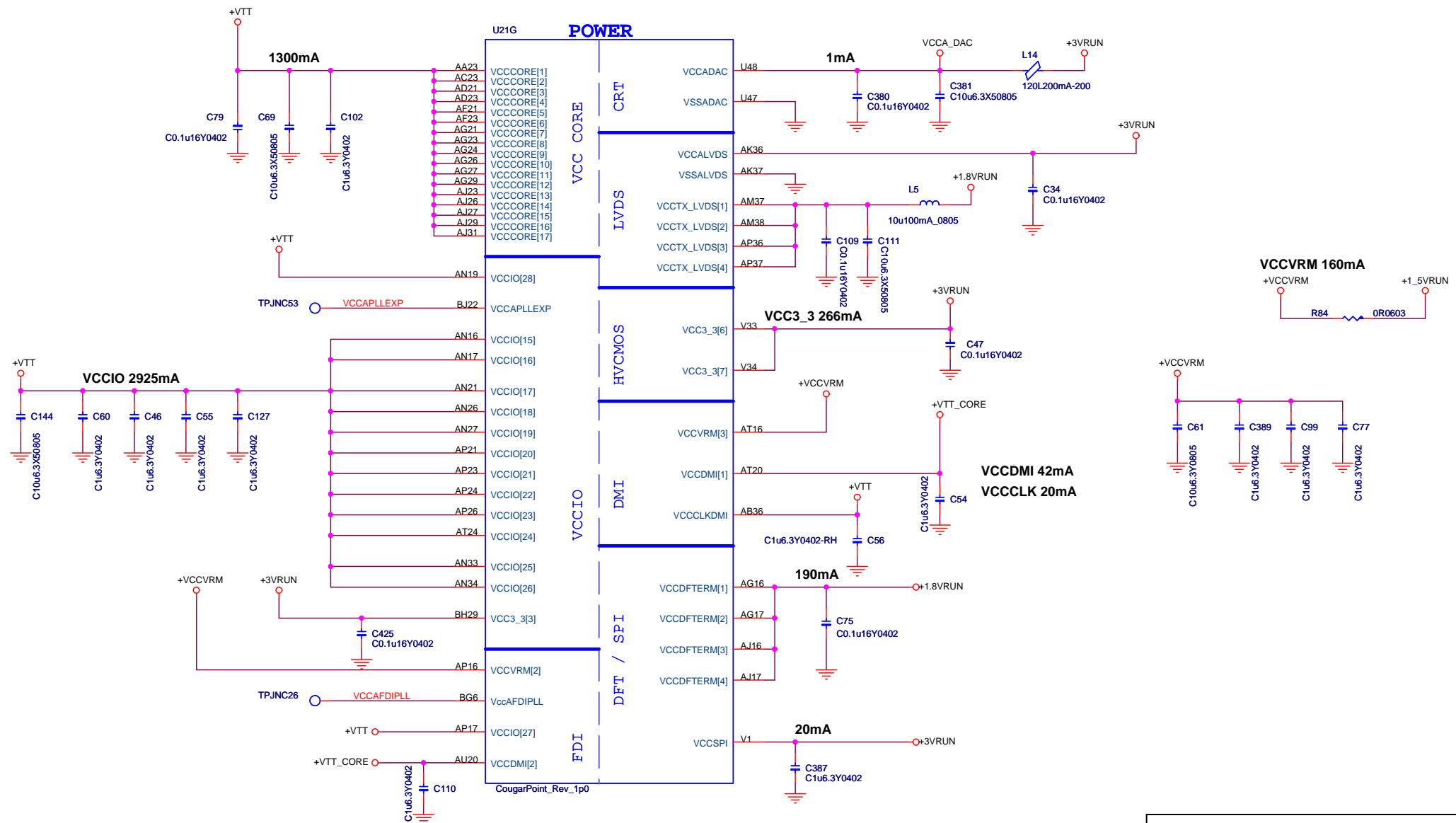


COUGAR POINT (GPIO,VSS_NCTF,RSVD)



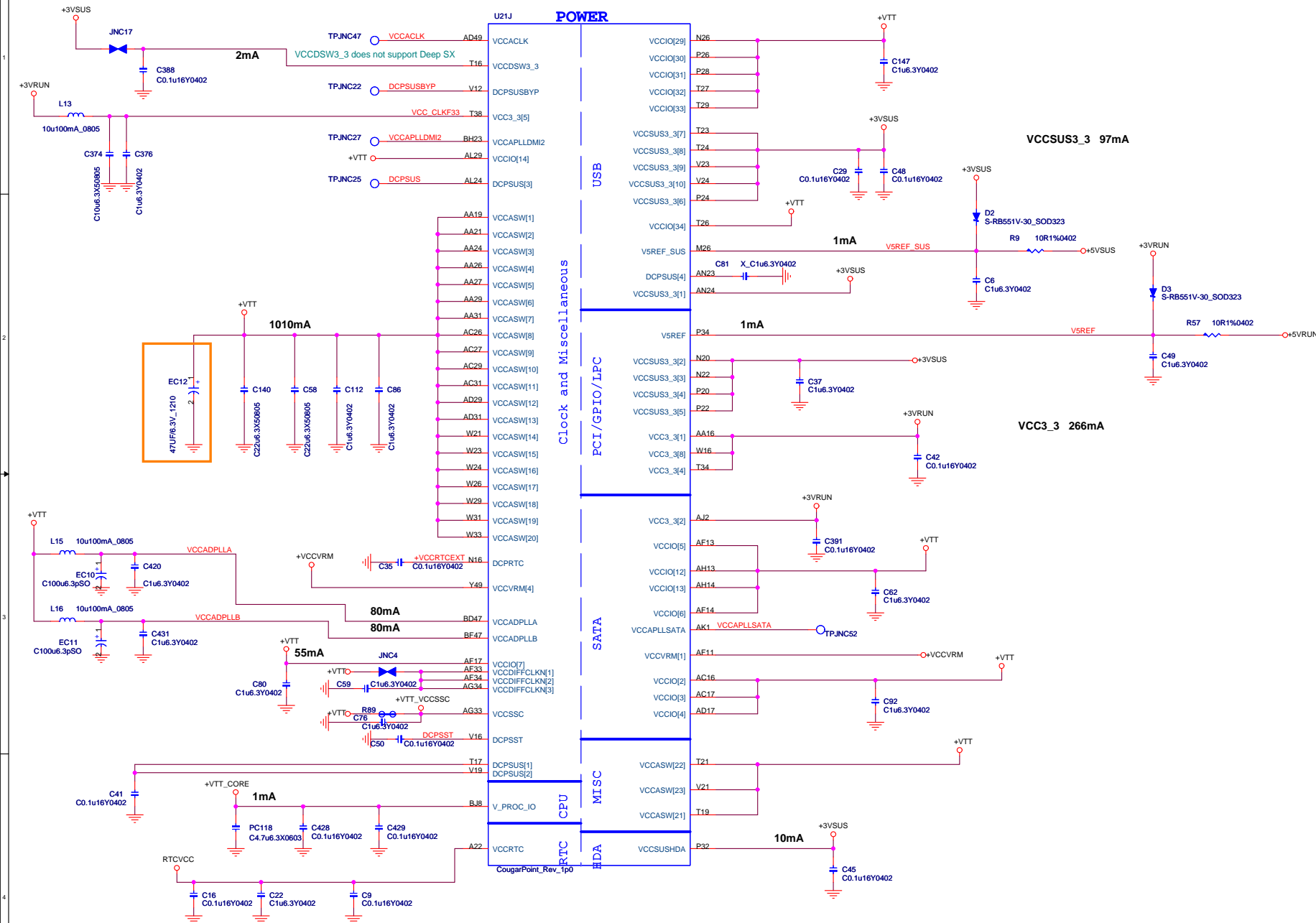
Title				
PCH-6 (GPIO/NCTF/RSVD)				
Size	Document Number			Rev
Custom	MS-16G3 / MS-16G5			0B
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COUGAR POINT (POWER)



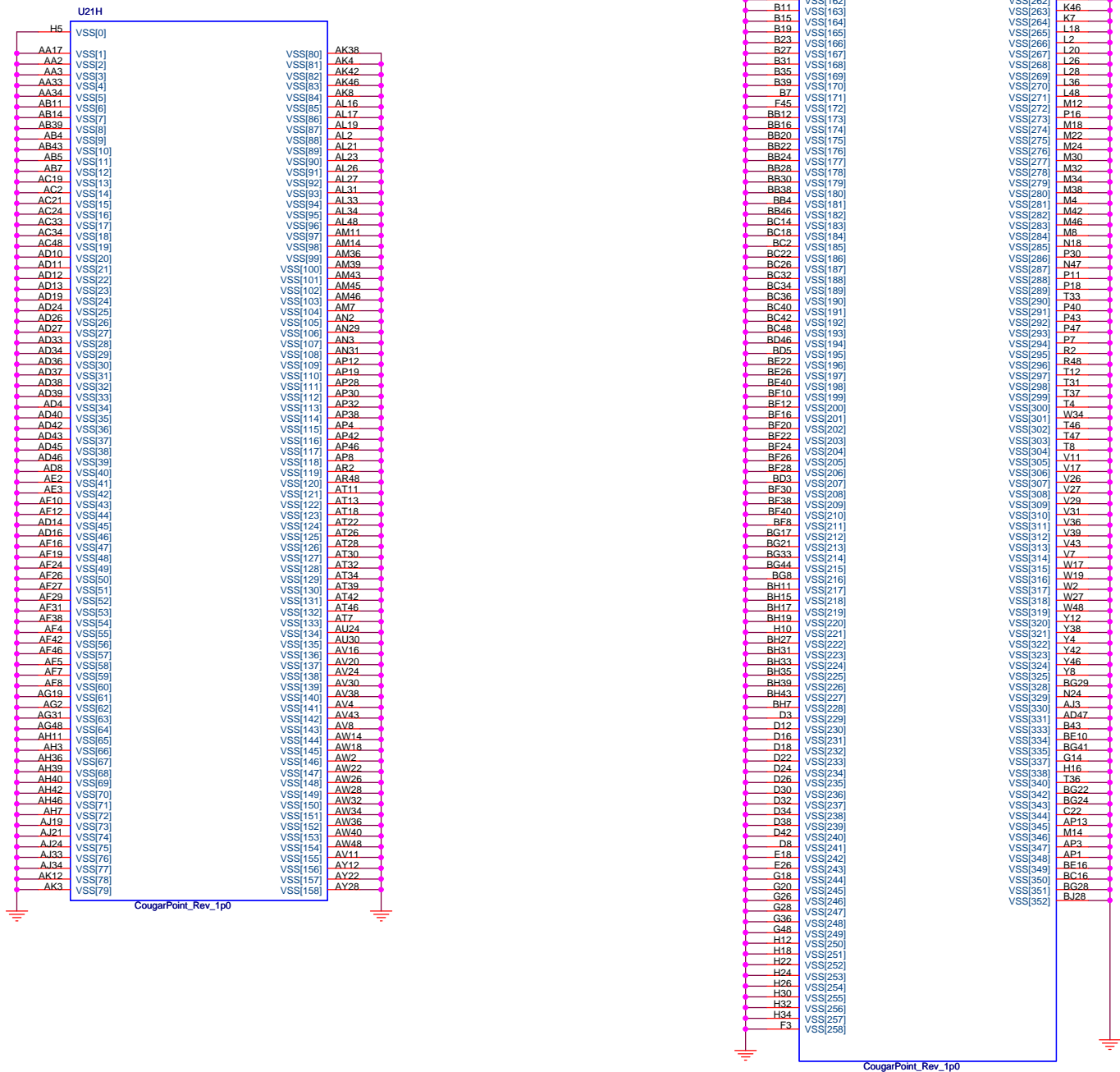
Title				
PCH-7 (POWER)				
Size	Document Number			Rev
Custom	MS-16G3 / MS-16G5			0E
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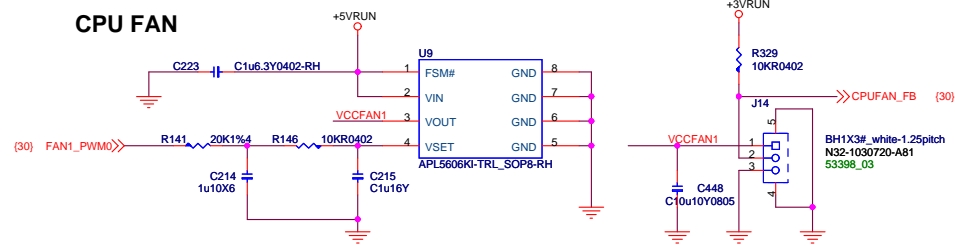
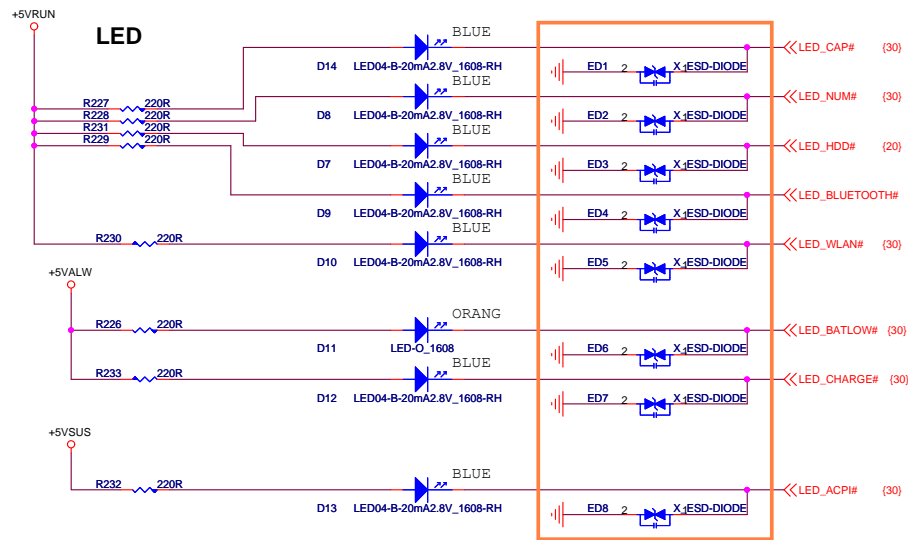
COUGAR POINT (POWER)



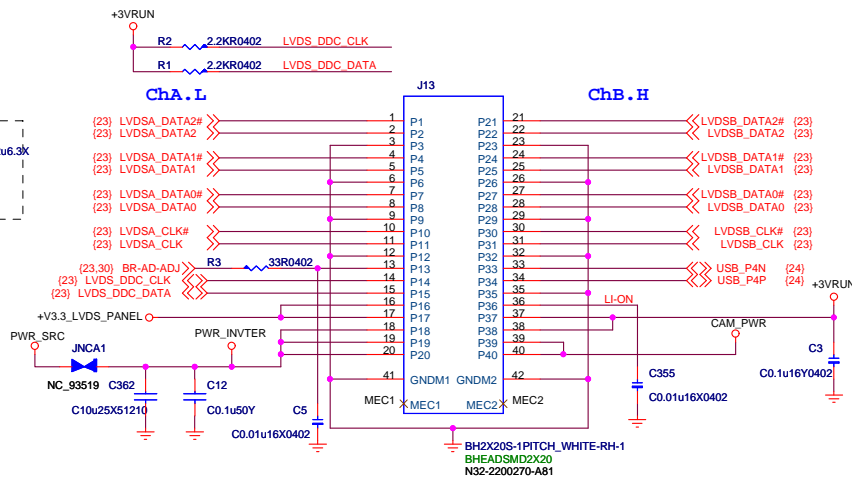
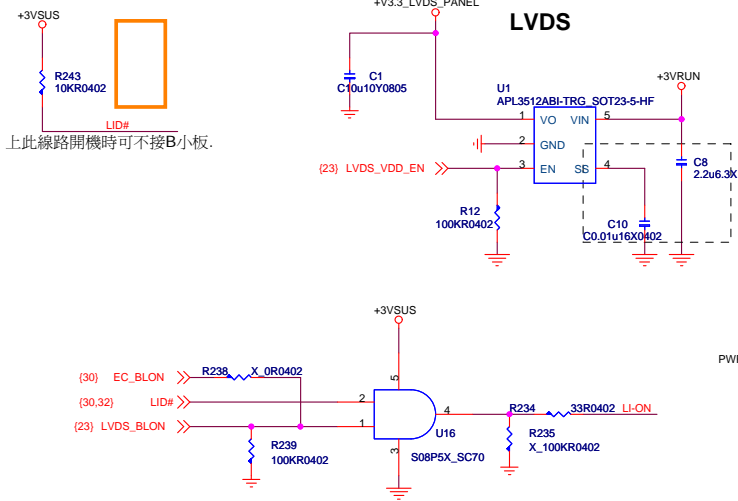
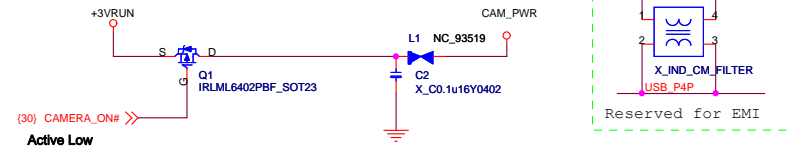
Title			
PCH-8 (POWER)			
Size	Document Number	Rev	
Custom	MS-16G3 / MS-16G5	OB	
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Cougar Point (GND)

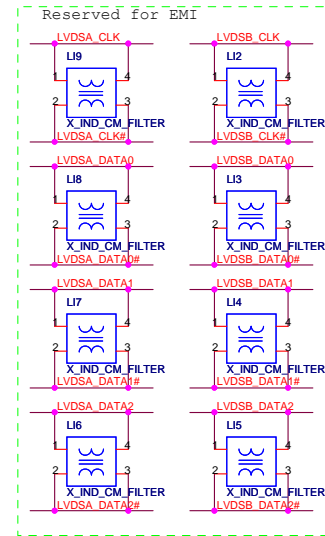





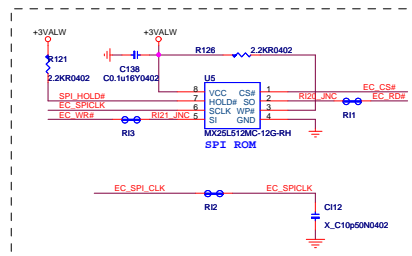
CAMERA



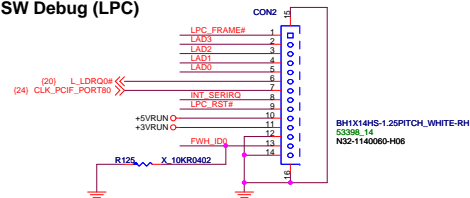
ChB.H



 MSI MICRO-STAR INTERNATIONAL CO., LTD.		MICRO-STAR INT'L CO.,LTD.	
Title			
FAN,LED, LVDS			
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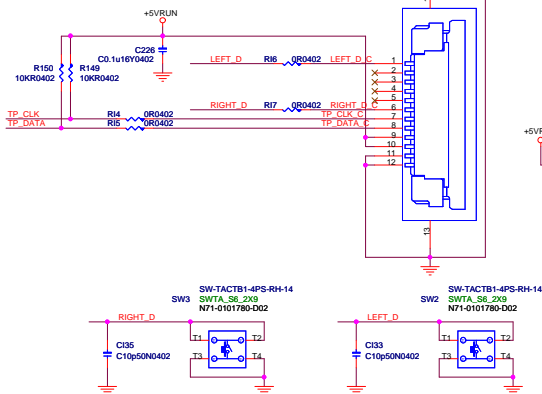
For SW Debug (LPC)



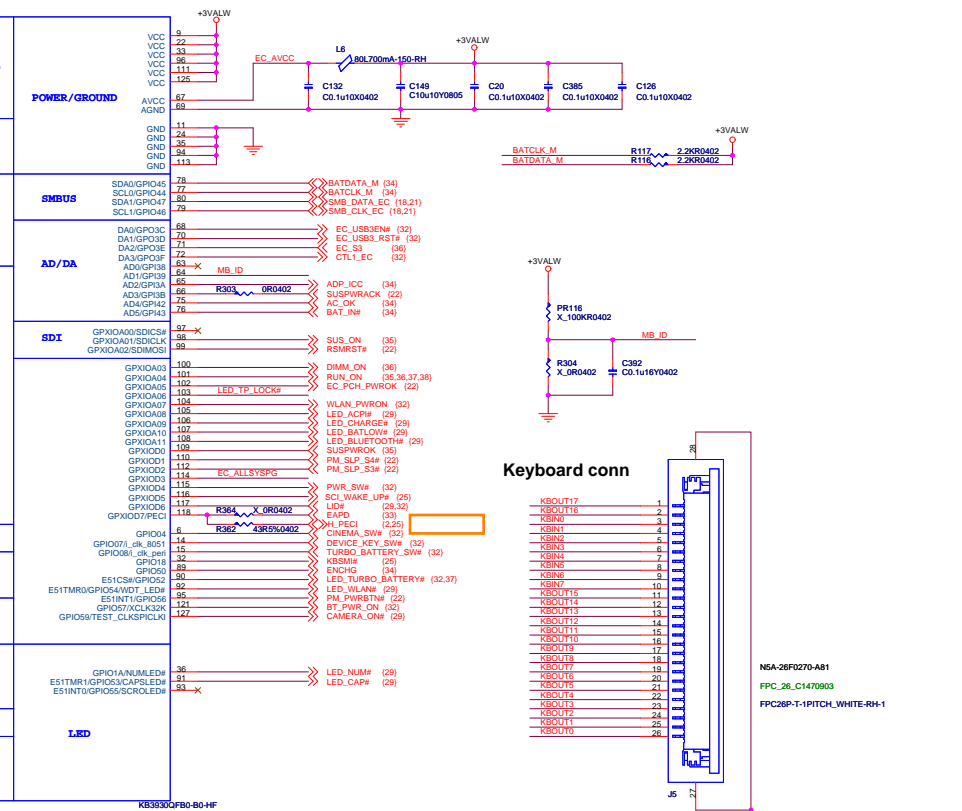
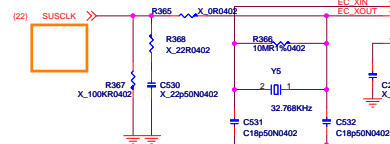
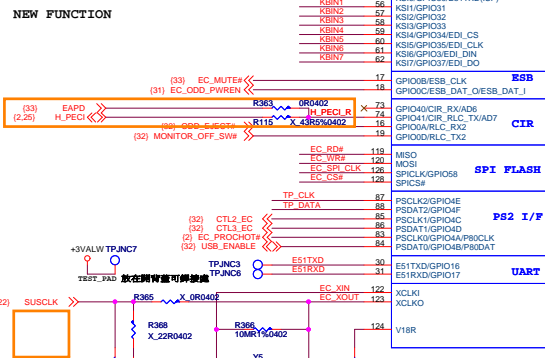
Touch Pad

Pin define follow MS-16GK Multi-Touch Pad

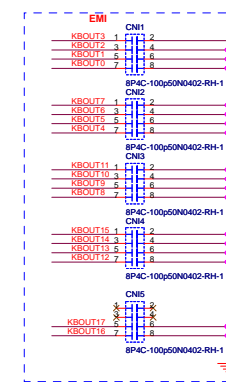
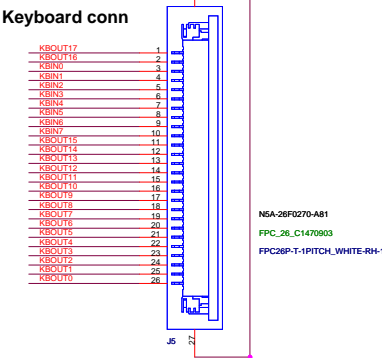
FPC12P-B-0.5PITCH_WHITE-RH-3
FPC_S12_3
N5A-12F0200-A81



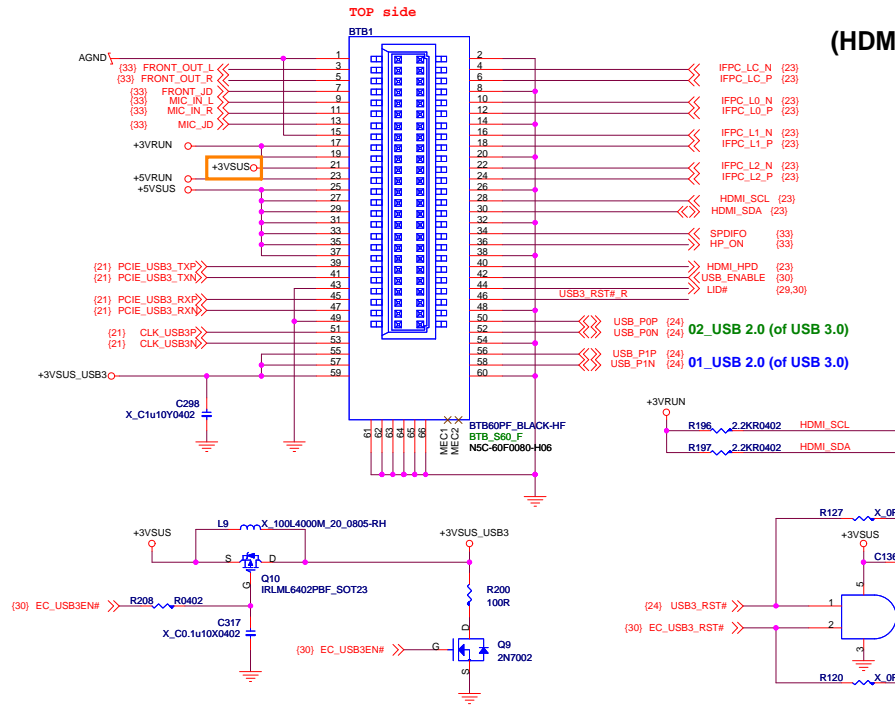
NEW FUNCTION



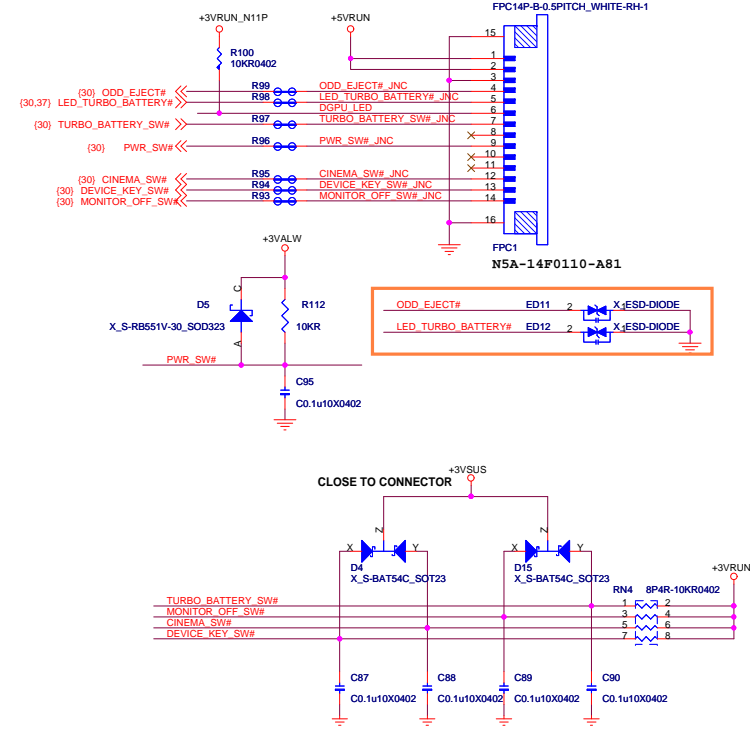
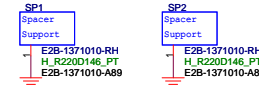
Keyboard conn



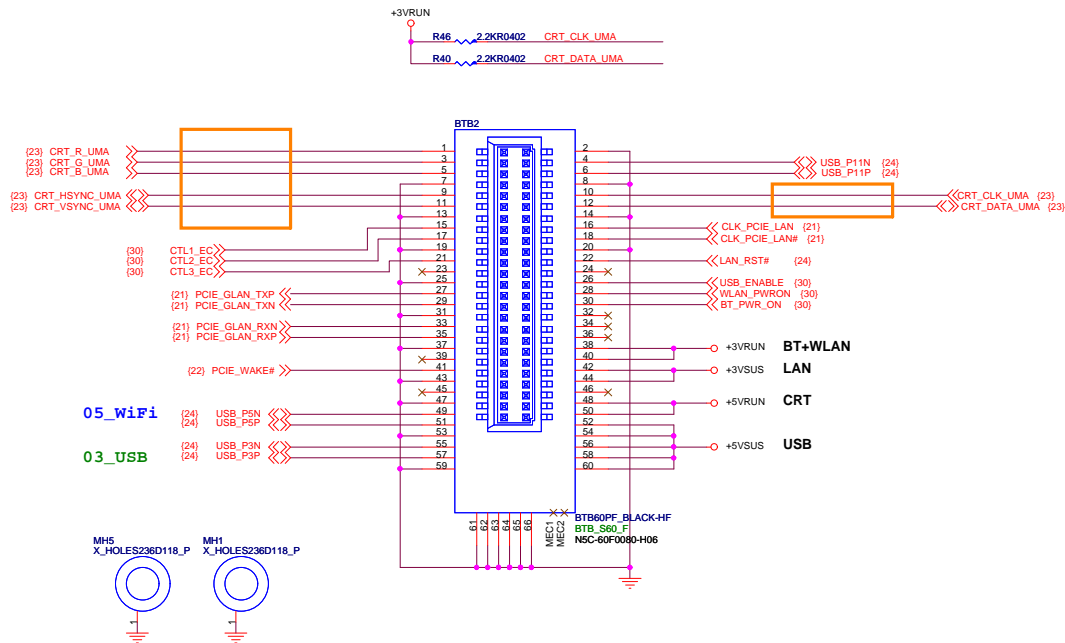
(HDMI,Audio,USB x 2)



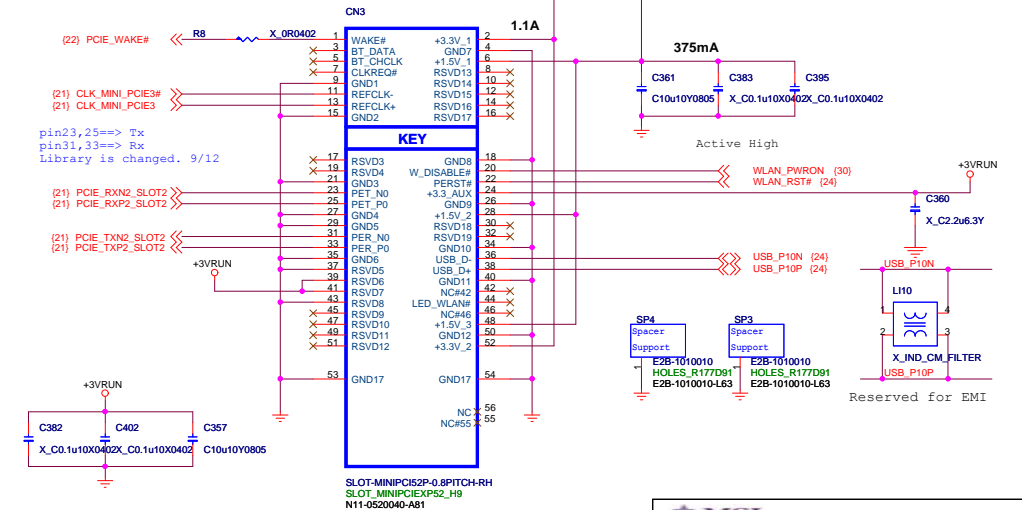
TOP side

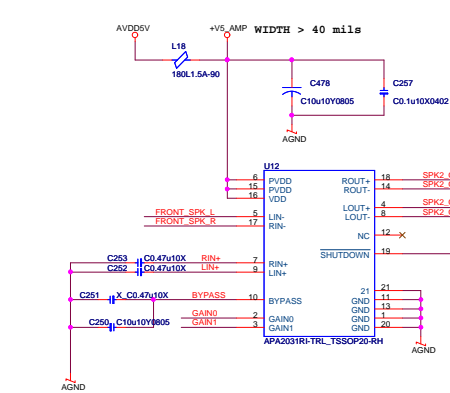
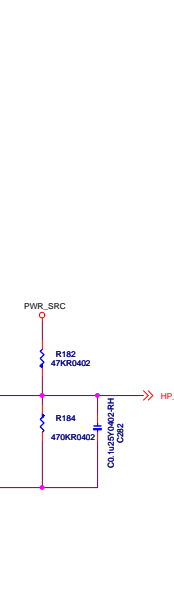
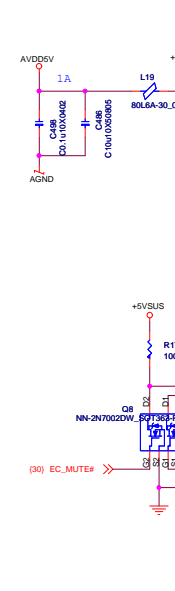
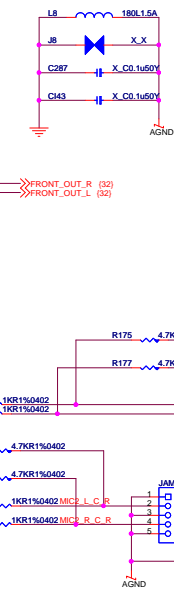
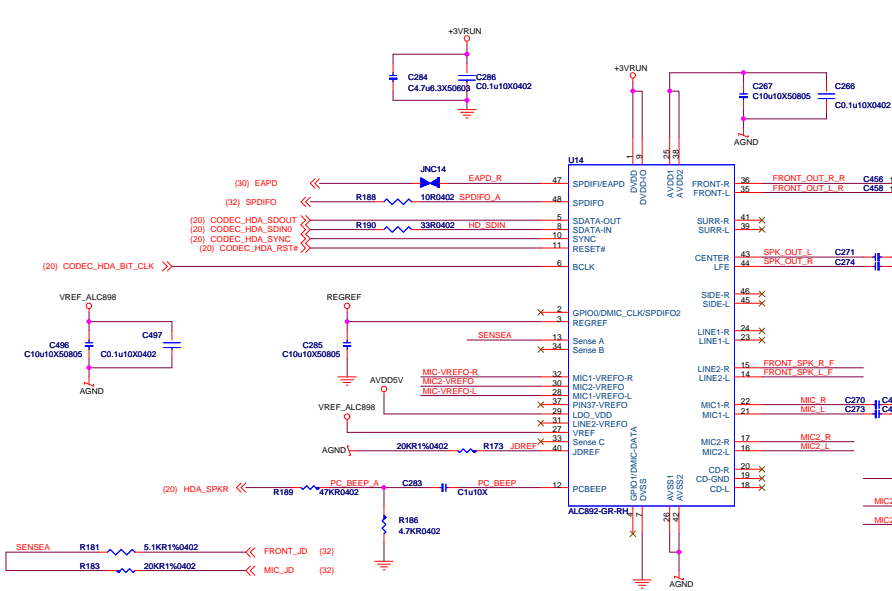


USB,LAN,CRT,BT+WLAN



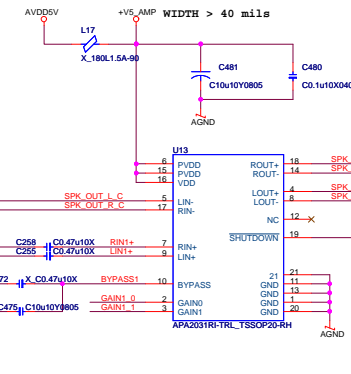
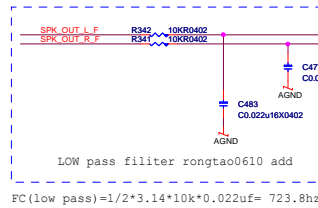
WLAN CARD



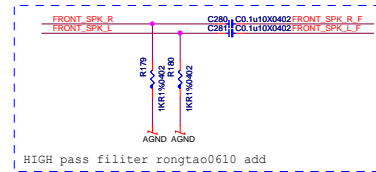
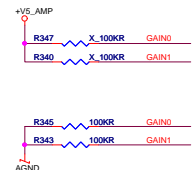


02/05 Change from PGND to DGND (include ALL PGND for Layout work)

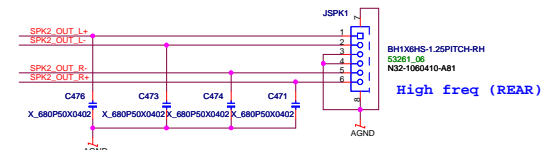
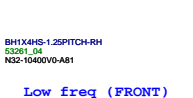
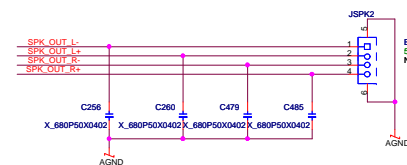
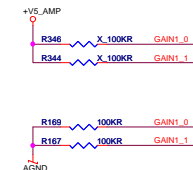
04/19 If stuff R166 and R508, R161 and R397 option one stuff.



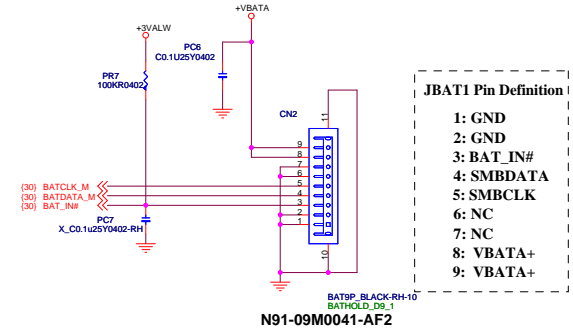
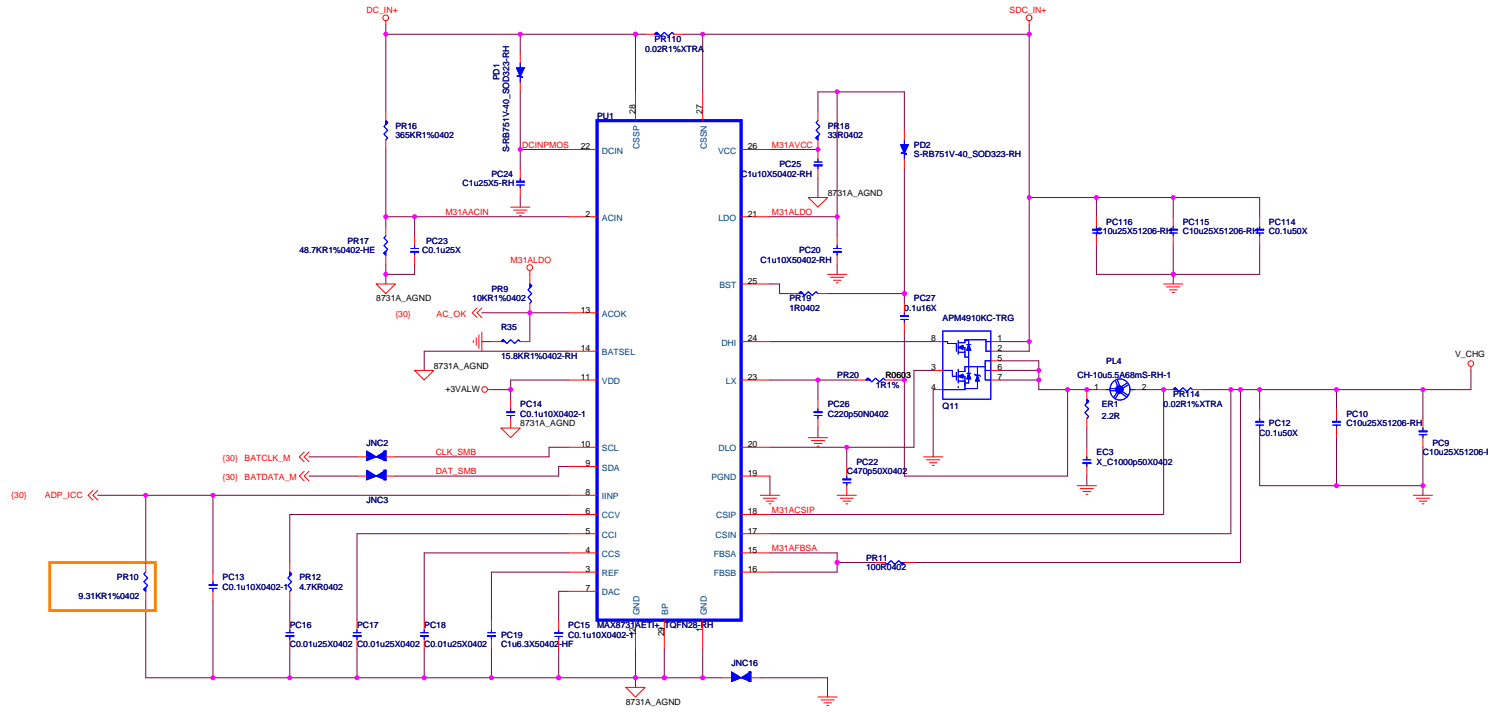
For APA2031				For FAN7031			
Av	GAIN0	GAIN1	SE/BTL#	Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0	6dB	0	0	0
10dB	0	1	0	10dB	0	1	0
15.6dB	1	0	0	15.6dB	1	0	0
21.6dB	1	1	0	21.6dB	1	1	0
4.3dB	X	X	1	4.3dB	X	X	1



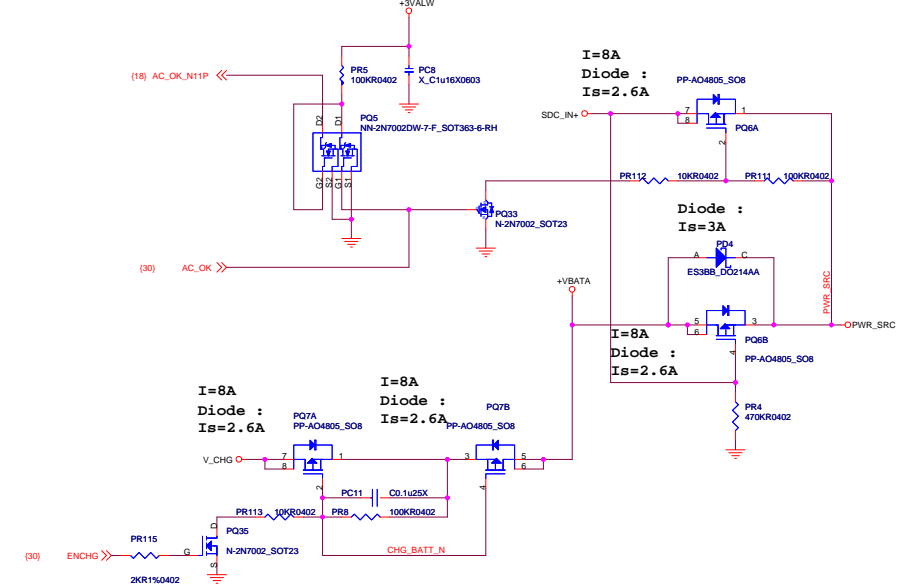
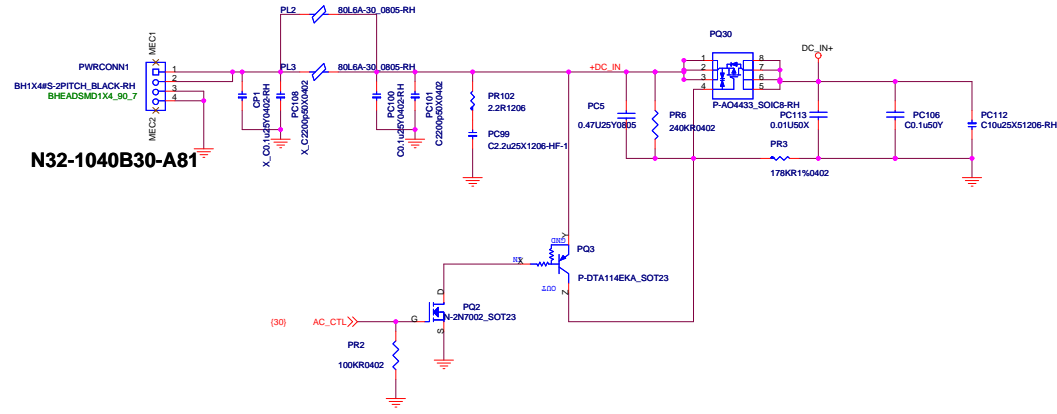
For APA2031				For FAN7031			
Av	GAIN0	GAIN1	SE/BTL#	Av	GAIN0	GAIN1	SE/BTL#
6dB	0	0	0	6dB	0	0	0
10dB	0	1	0	10dB	0	1	0
15.6dB	1	0	0	15.6dB	1	0	0
21.6dB	1	1	0	21.6dB	1	1	0
4.3dB	X	X	1	4.3dB	X	X	1

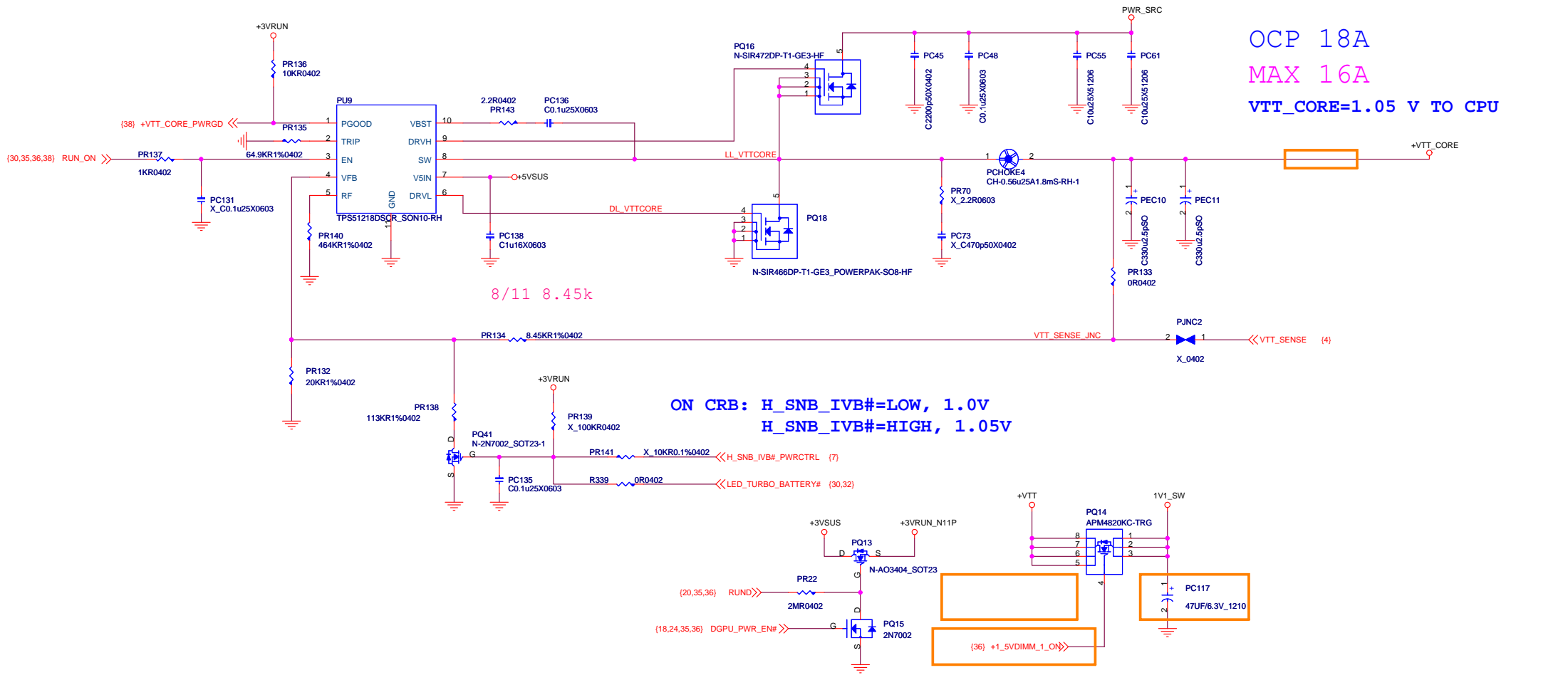


Adapter input voltage set 19 Voltage



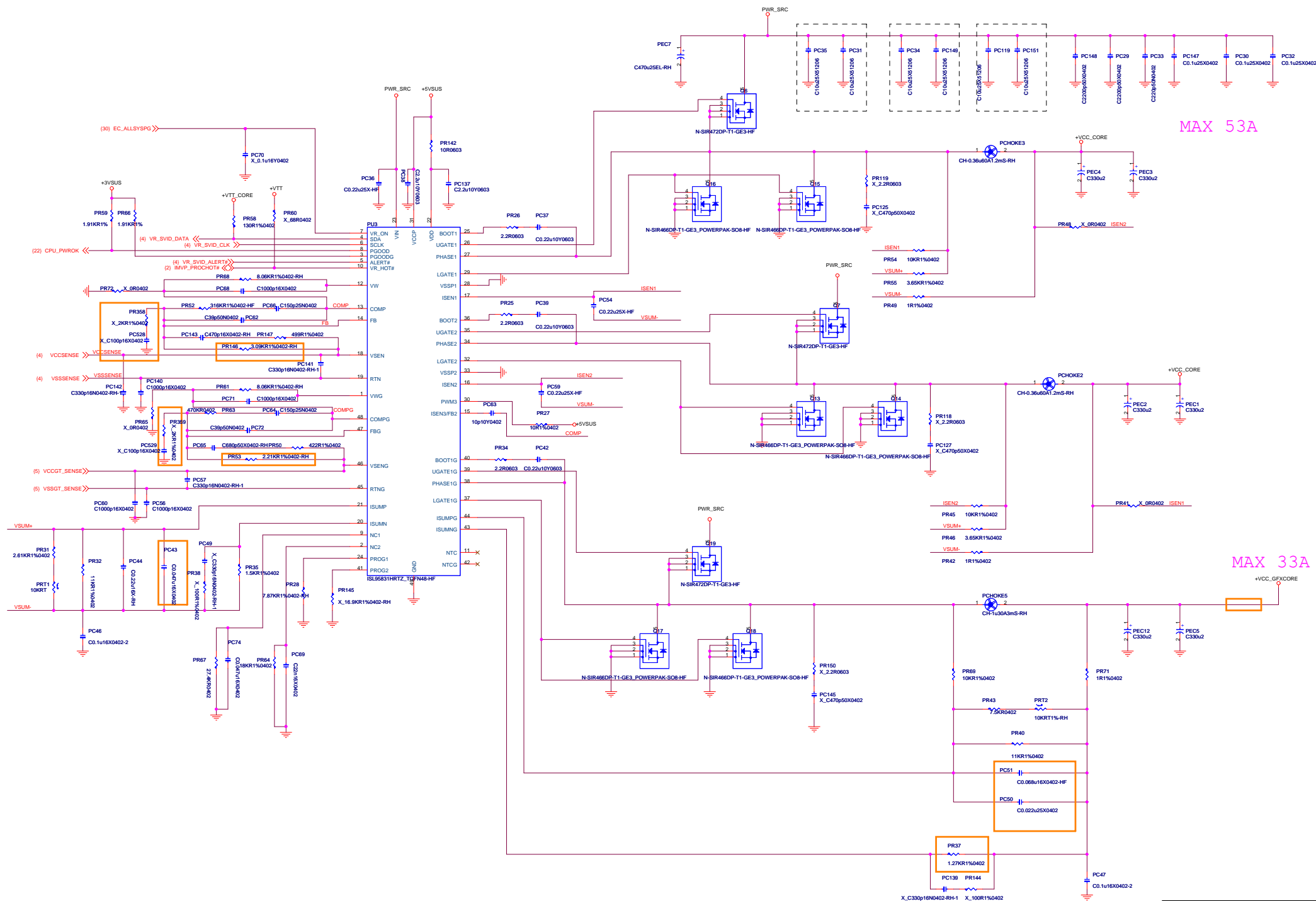
IINP :
1. The transconductance from (CSSP - CSSN) to IINP is 3mA/V.
2. $V_{IINP} = IINP \times R_{S1} \times 3mA/V \times PR25$





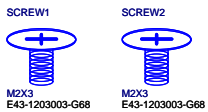
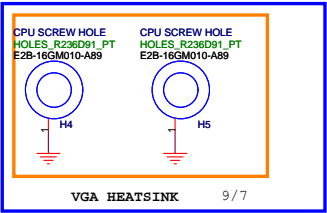
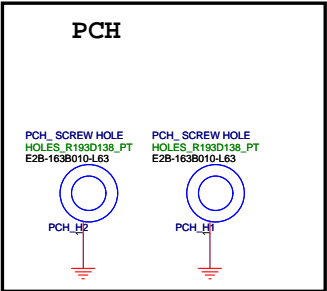
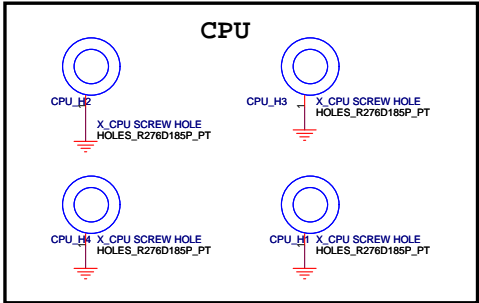
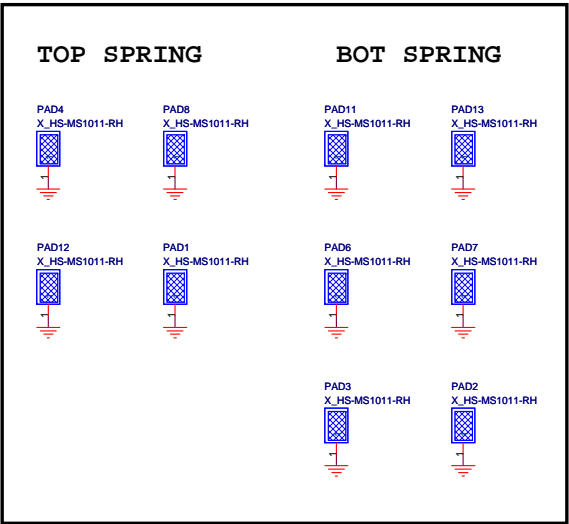
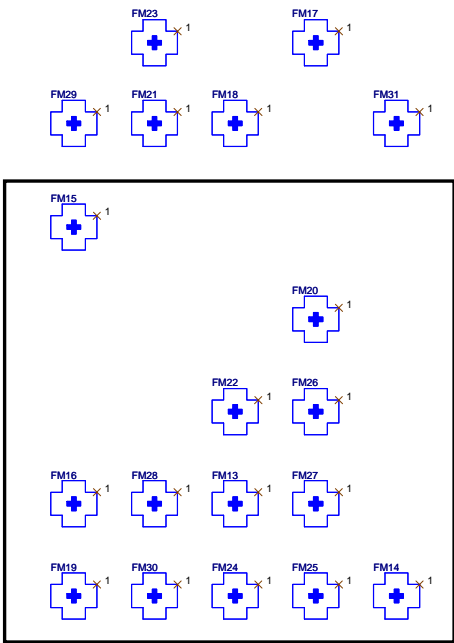
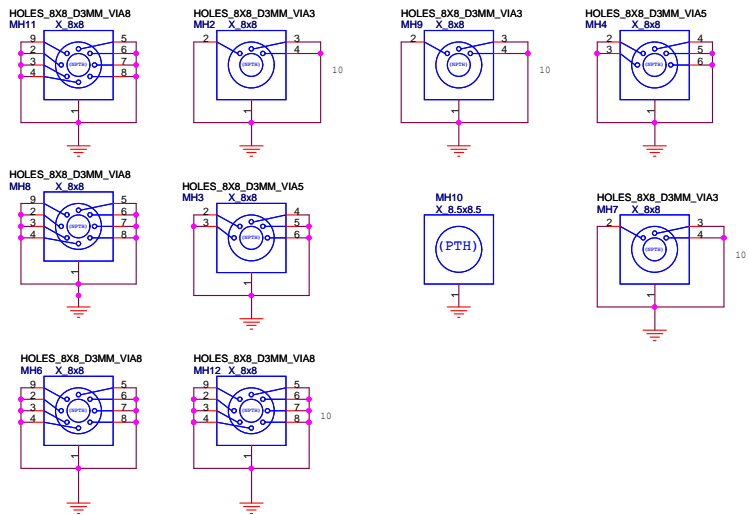
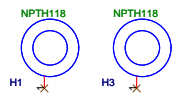
OCP 18A
MAX 16A
VTT_CORE=1.05 V TO CPU

ON CRB: H_SNB_IVB#=LOW, 1.0V
H_SNB_IVB#=HIGH, 1.05V

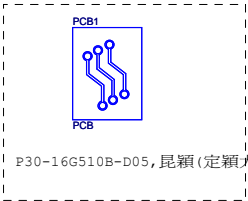
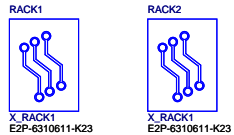


MAX 53A

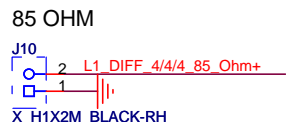
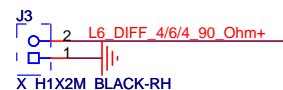
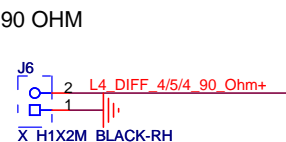
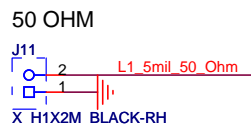
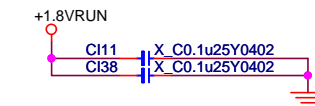
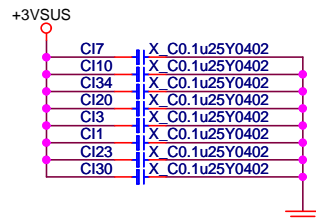
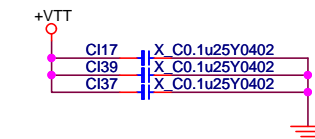
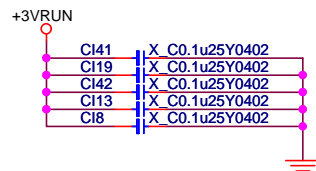
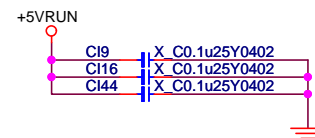
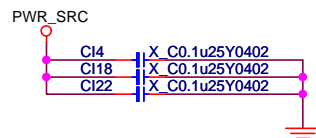
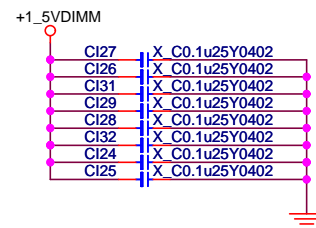
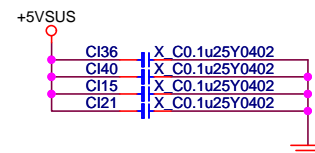
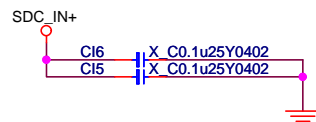
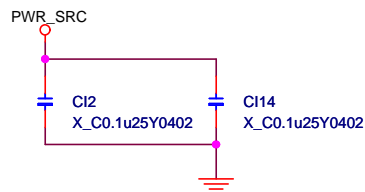
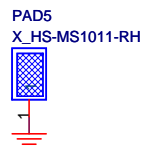
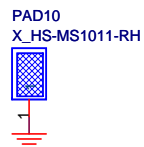
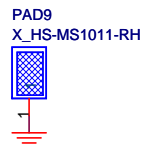
MAX 33A




04/20
ADD SB Heatsink and Screw x2

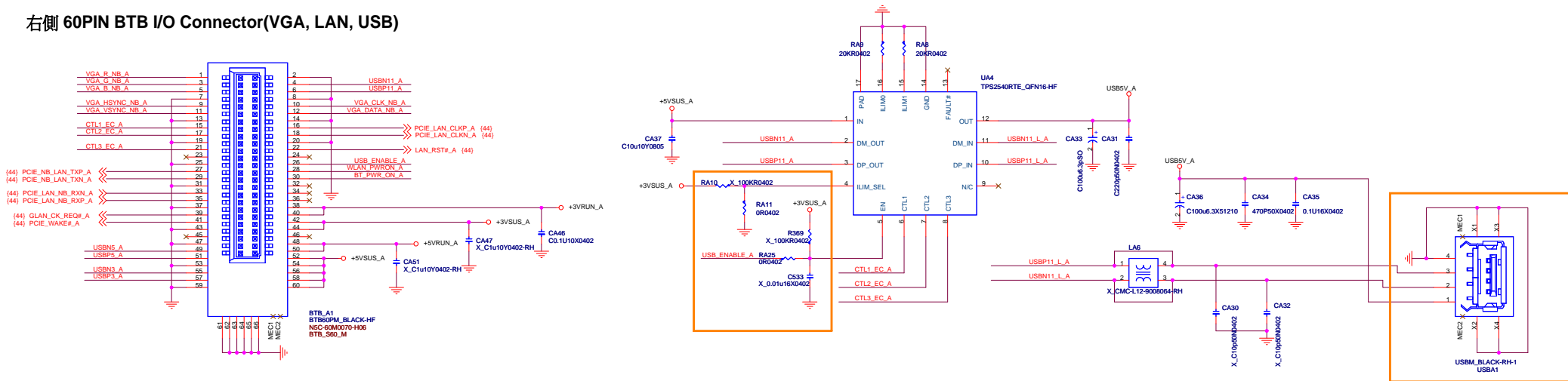


BOT SPRING

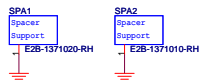


 MICRO-STAR INT'L CO.,LTD.	
Title	
EMI	
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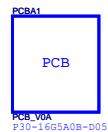
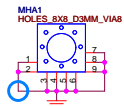
右側 60PIN BTB I/O Connector(VGA, LAN, USB)



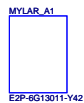
**BTB STANDOFF
(16GMA)**



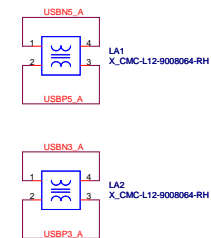
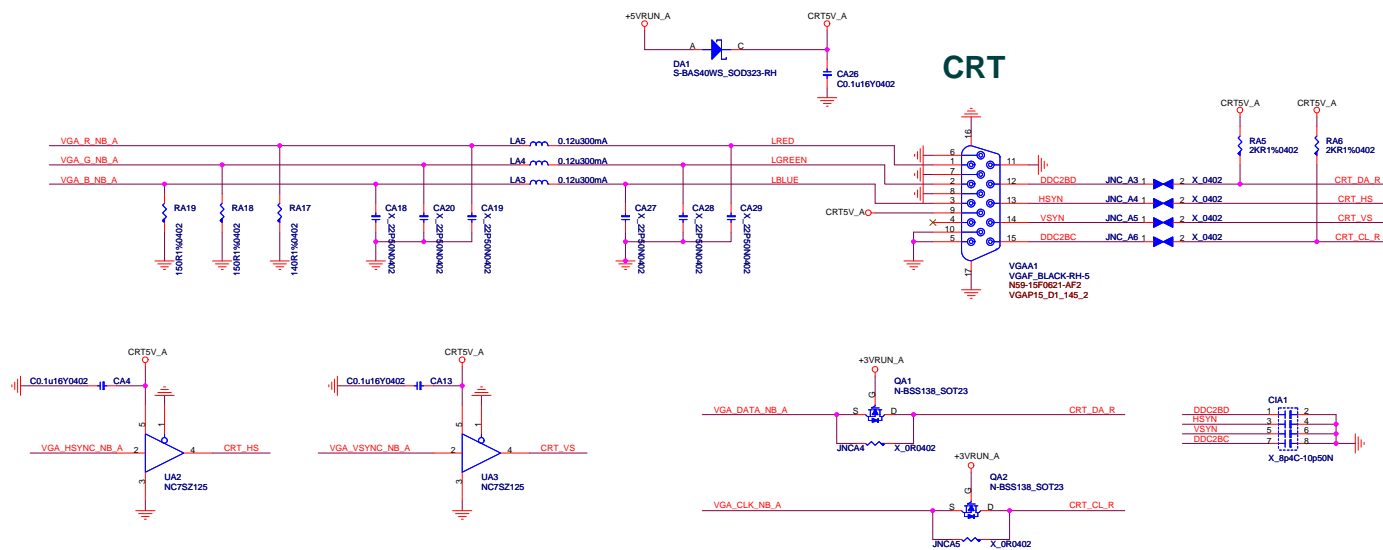
SCREW HOLE



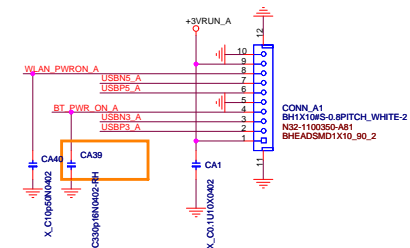
Mylar for M/E
ASM CFG = 60

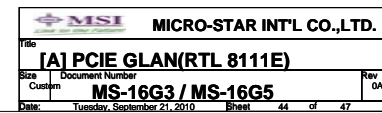


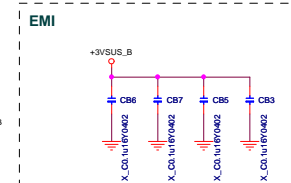
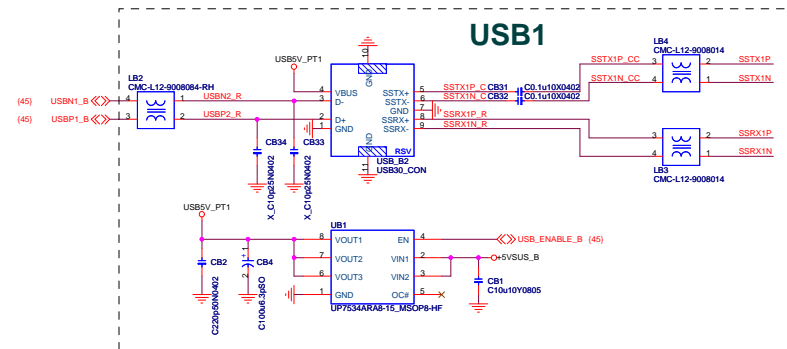
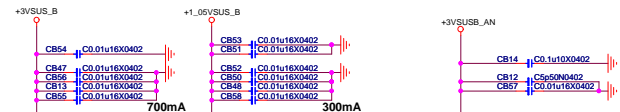
CRT

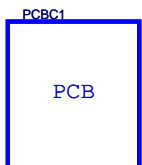
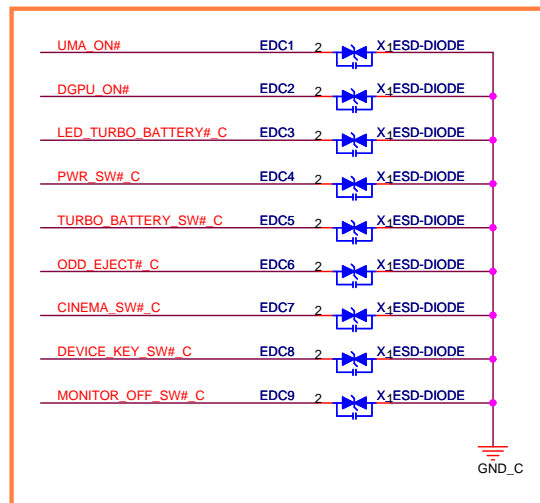
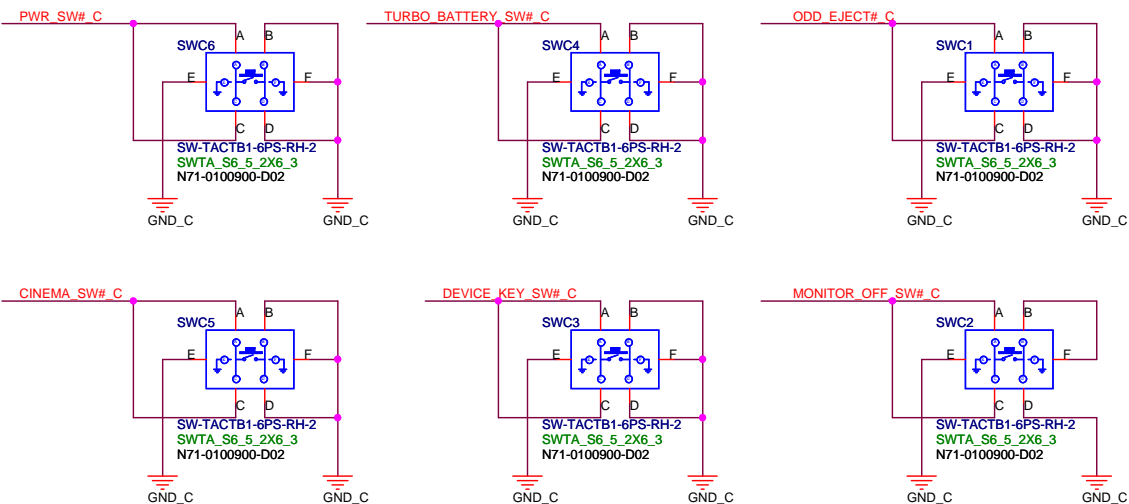
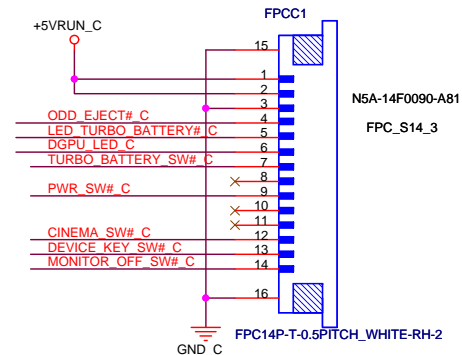
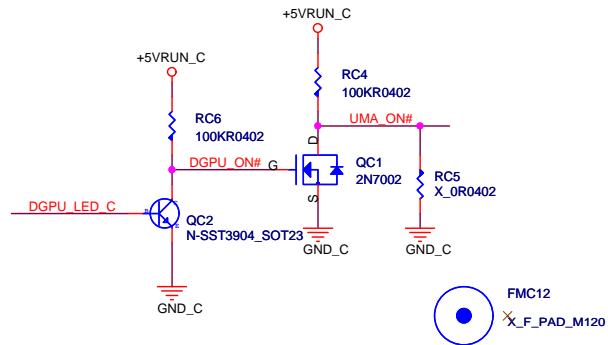
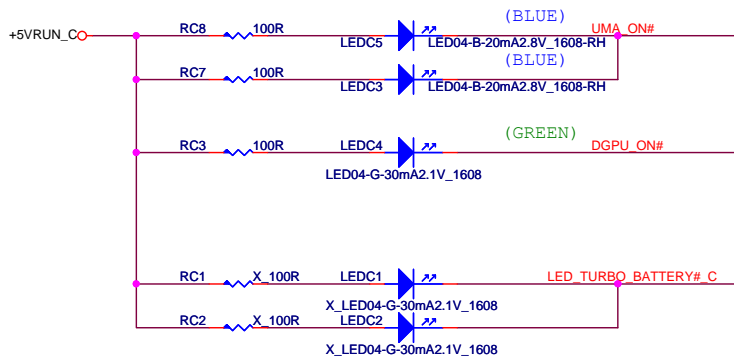


BT+WLAN Combo



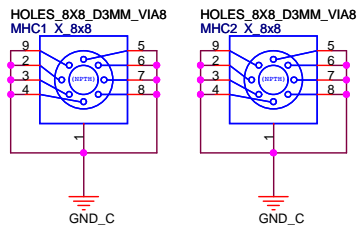






PCB_V0A
P30-16G5C0B-D05

P30-16G5C0A-D05,昆穎(定穎大陸),



02/10 Add 8 vias for EMI sugesstion

MSI		MICRO-STAR INT'L CO.,LTD.	
Title		[C] PWR SW /LED Launch Board	
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